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Using an Advanced Signoff Methodology on high performance designs to reduce OCV margins.

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Design Example: ARM® CORTEX™-A8S Processor

Support for ARMv7

- Added new support for Thumb®-2, Jazelle®-RCT and NEON™

In-Order Superscalar Pipeline

- 2.0 DMIPS/MHz
- 1 GHz in TSMC90G

High speed Level 1 Caches (16K or 32K)

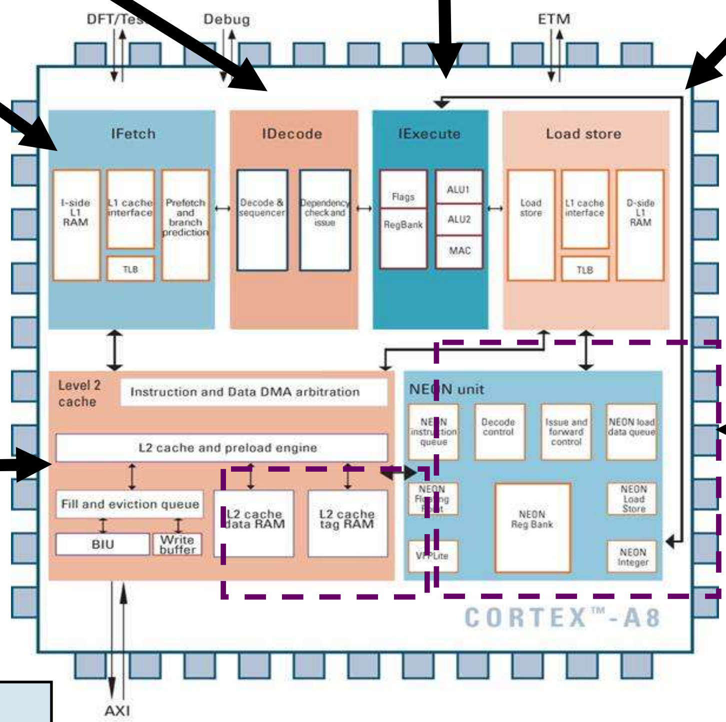
- Dual 32 entry TLB
- Minimized access time maximizes throughput to main memory
- Controlled array access minimize power consumption

Advanced Dynamic Branch Prediction

- 95% accurate across industry benchmarks

Integrated L2 Cache (0K, 64K – 2M)

- Optimizes access to larger data sets and minimizes bus traffic
- AXI bus to system memory and peripherals
- L2 Preloading Engine for larger data sets



Dedicated NEON unit for media and signal processing

- 2 to 10x performance improvement
- Integer and Floating Point support

400k placeable instances after synthesis

8.55mm2 in TSMC 65LP

Background.

- Originally designers added margin to their design using clock uncertainty. This would model all paths as having the worst possible timing.
- Then designers pulled out some of this global design margin in the form of OCV for the worst case and best case library corners.
- This is too pessimistic for the smaller process nodes such as 65nm and 45nm.
- If the local effects of IR drop at each instance are taken into account then the global OCV margin can be reduced.
- The approach outlined here uses dynamic power analysis of the power supply grid in VoltageStorm® Dynamic Gate, using dynamic test vectors to determine the actual IR drop of each instance to feed into the Signoff STA.
- Static timing analysis can then check that the design is still operational at the worst case IR drop conditions for the power supply grid.

Flow Methodology.

1. Determine the worst case vectors for max activity and max power consumption. Run simulations using a suitable test bench to generate a VCD file for the design. This is done using the NC-Verilog® simulator.
2. Extract the design parasitics using Cadence® QRC Extraction for the required process corners. Generate the Timing Window File, (TWF), using the Encounter® Timing System, (ETS).
3. Read the DEF file, Timing Window File, design constraints, parasitics and the VCD file into Powermeter to produce the dynamic instance power values.
4. Run VoltageStorm® Dynamic Gate to analyze the power grid dynamically using the Powermeter instance power values and convert them to instance IR drop values for STA.
5. Finally, run Static Timing Analysis using ETS and read in the IR drop files generated by VoltageStormPE™.
6. Analyze the timing paths in ETS.

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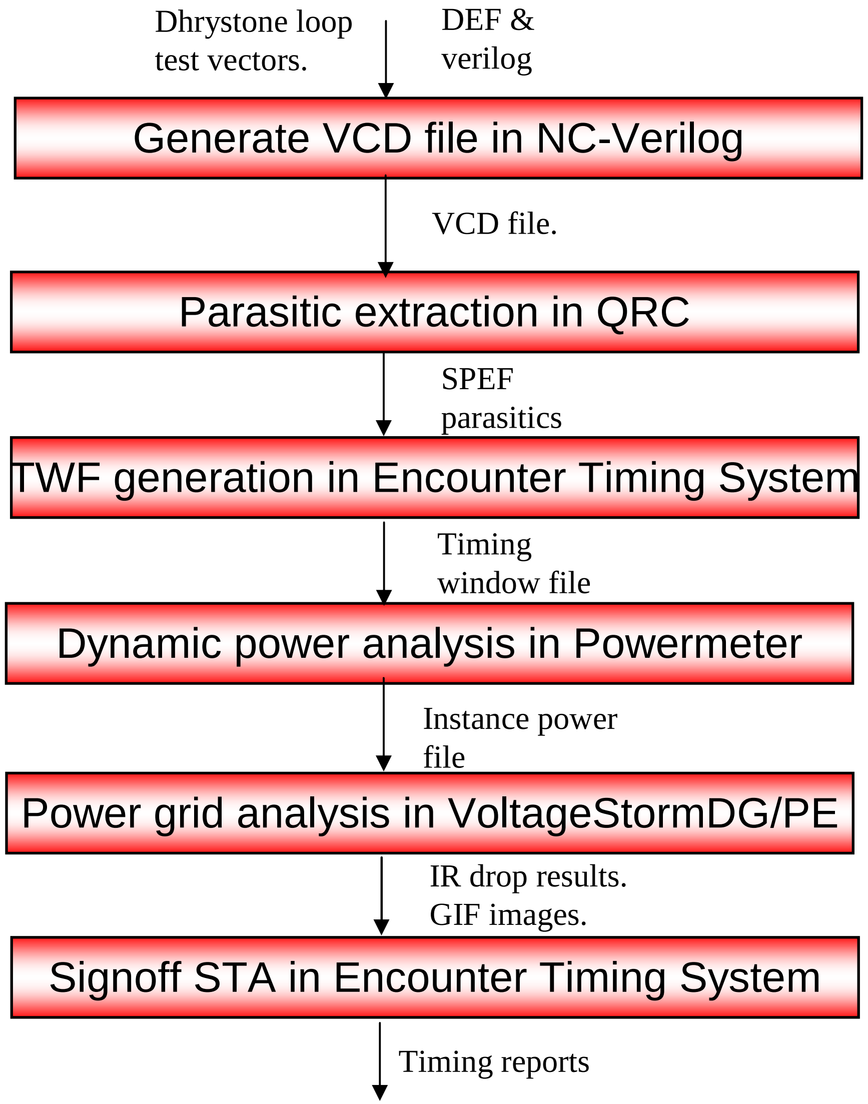
Advanced Signoff flow diagram.



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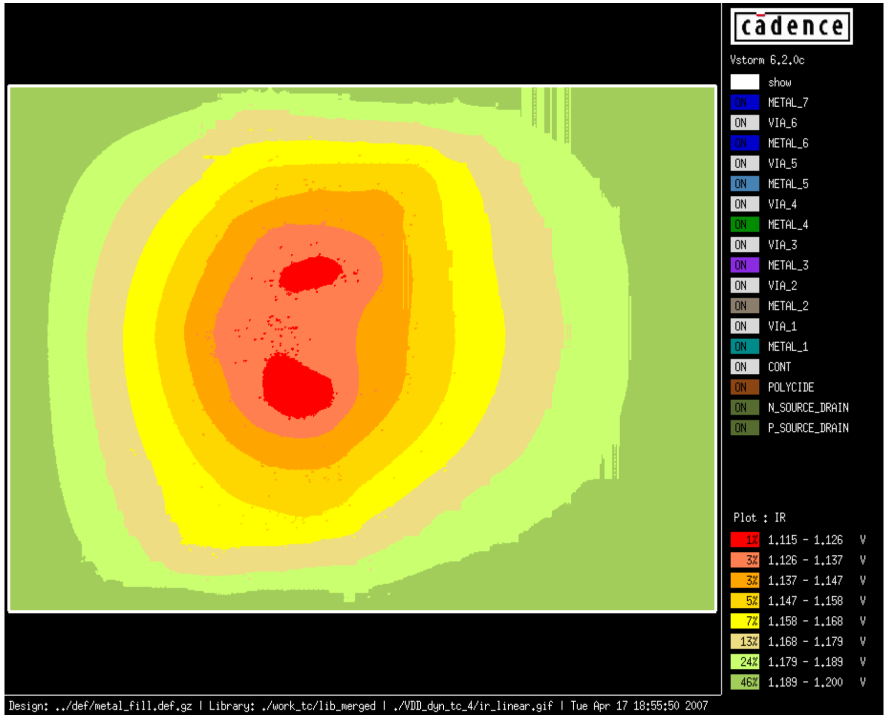
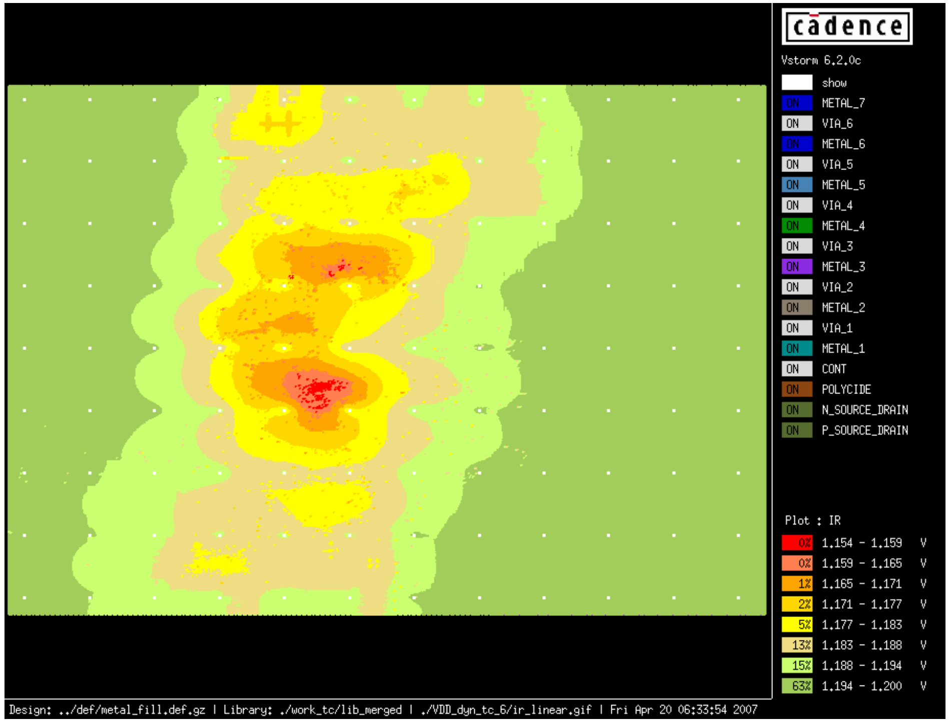
IRdrop affects gate delay.





- Voltage supply points are all around the design edges. This results in a high IR drop and timing is degraded.
- Voltage supply points are spread over the design using a regular array of “bumps” on the highest metal layer. This results in a much lower IR drop.

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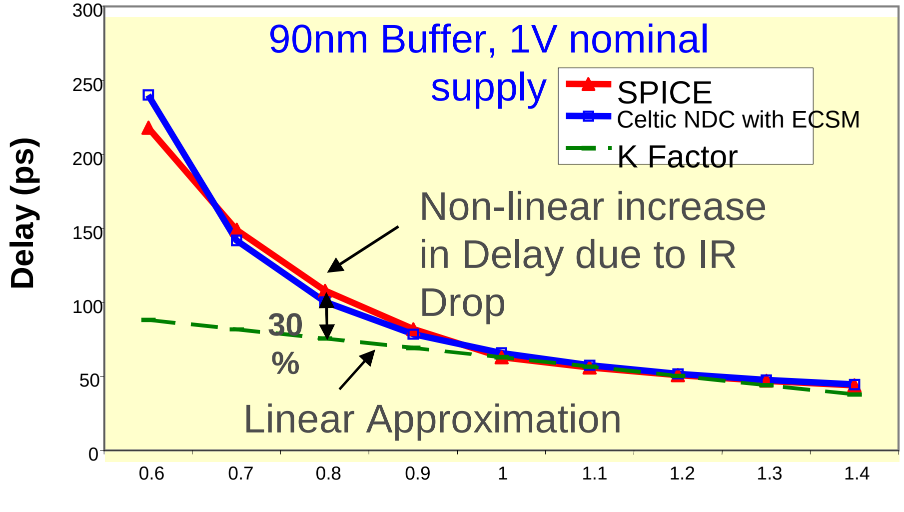
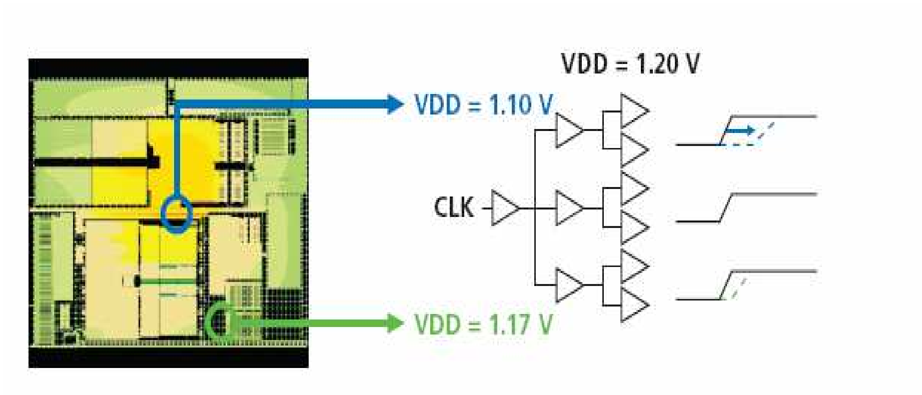
IR Drop Impact on delay.



IR Drop Impact on Delay



Relation of IR drop to skew and subsequent timing violations

Conclusions.

- Design margins can be reduced by accounting for physical effects such as IR drop directly, rather than as part of OCV. This reduces over constraint and therefore improves design closure time and secondary effects such as power consumption and area.
- Use worst case power vectors to run a dynamic power analysis in VoltageStorm DG to generate the instance IR drop values.
- Include the IR drop instance values in the STA using ETS.
- Use ECSM timing extensions for improved accuracy during the STA.