

Altera Stratix GX Design-in Kit for Cadence Allegro Platform

To solve the challenges of implementing multi-gigabit serial links, Cadence worked with Altera as they developed this design-in kit that is available through Altera sales representatives. The HTML based kit walks the user through a methodology on how to design-in the Stratix GX HSSI SerDes transmitters and receivers.

Included in the methodology is signal integrity analysis of high-speed differential serial links running at speeds up to 3.125 Gbps using Cadence Allegro SI behavioral DML models. These models have been validated against Altera transistor-level models, but run hundreds of times faster. Also included in the kit are ready-to-run topology files, PCB reference files, footprints, tutorials, documentation, scripts, and other utilities, giving you everything they need to quickly and easily bring your designs featuring Stratix GX to market. To learn more about the Stratix GX architecture, visit the Altera website.

Customers are able to request the kit by submitting a Product Related Service Request.

This silicon design-in kit includes all you need to perform serial link simulation with Altera's FPGA at either end of your PCI Express link. To learn more about this kit and others, download the PCI Express design chain kits.