

## **Intel Chipsets design-in kit for PCI Express**

A part of the PCI Express design chain is the PCI Express silicon design-in kit for Intel's 915 and 925X Express chipsets. This silicon design-in kit includes all you need to perform serial link simulation with Intel's chipset at either end of your PCI Express link. Cadence and Intel have correctly staged Intel's behavioral model data in the Cadence DML MacroModel format such that simulation results match those of Intel's transistor-level models, but run hundreds of times faster. Also included in this kit, you will find ready-to-run topologies in Cadence Allegro PCB SI format that represent Intel's Golden Channel model for PCI Express simulation.

In addition, as in the past, Intel will also provide a Cadence Allegro platform drop-in core layout (DCL) for the Grantsdale chipset. A DCL will reduce the design cycle by weeks by leveraging Intel's engineering investment in designing this core compliant with complex design rules associated with critical busses and interfaces. To learn more about this kit and others, download the [PCI Express design chain kits](#).