



IBIS Models for High-Speed Interfaces

Lynne Green

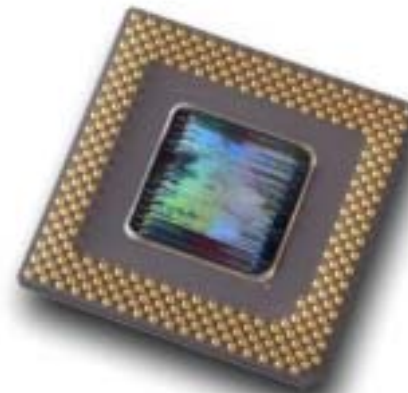
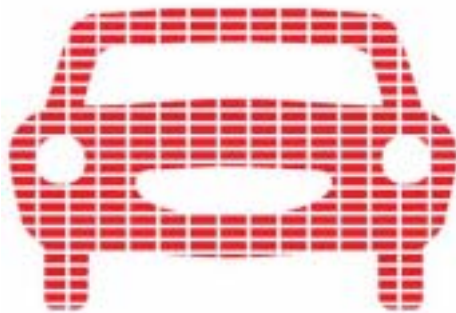
March 2003

Overview



- Model Creation
- Differential Models
- Validation Methodology
- On-die Terminators
- LVDS Model Example
- High-Speed Interconnect Models

High-Speed Designs Require Analysis



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EIA/ANSI 656-A

I/O Buffer Interface Specification

- Publicly available parser
 - IBIS 3.2.9 parser today
- Version 4.0 voted in 2002
 - IBIS 4.0 parser Q2/2003
- Version 4.1 in development
 - Support for SPICE and AMS models
- Interconnect spec in draft
 - Includes S-parameters

EIA/ANSI 656-A IBIS Quality Committee



- Requirements for accuracy and completeness
- Quality levels
 - Level 0 Software checks
 - Level 1 Add visual checks and other features
 - Level 2A Comparisons to simulation data
 - Level 2B Comparisons to test bench data
 - Level 3 Both 2A and 2B
- Requesting revisions to specification and parser

Component description

Model Assignment



[Pin]

! Pin name	Model	Name
D1	IO_1	Single-ended I/O
DD1	IO_1	Differential I/O, non-inverting
DD2	IO_1	Differential I/O, inverting
4	In1	Diff input, non-inverting
5	In1	Diff input, inverting
6	In1	Single-ended input
9	GND	Ground pin #1
10	GND	Ground pin #2
11	POWER	Power Pin #1
12	POWER	Power Pin #2

Component description

Pin association



[Diff Pin]	inv_pin	vdiff	tdelay_typ	tdelay_min	tdelay_max
DD1	DD2	NA	-1.0ns	0ns	0.1ns
4	5	150mV	NA	NA	NA

[Series Pin Mapping]	pin_2	model_name	function_table_group
4	5	Rser1	Series Resistor, always ON
DD1	DD2	MOS1	1 Series Resistor, two values

[Series Switch Groups] | Function Group States

On 1

Component description

Pin association



| For SSN analysis

[Pin Mapping]	pdn_ref	pup_ref	gnd_cl_ref	power_cl_ref
DD1	9	11	9	11
DD2	9	11	9	11
D1	9	11	9	11
4	10	12	10	12
5	10	12	10	12
6	10	12	10	12

Component description

Programmable buffers



| IO_1 has programmable drive current strength

[Model Selector] IO_1

| first one is the default model

INOUT_4 | 4 mA buffer without slew rate control

INOUT_4S | 4 mA buffer with slew rate control

Model Creation

Obtaining parameters

- Data sheets
 - Logic interface
 - Temperature
 - Single/dual voltage operation
 - Thermal coefficients

- Estimating die temperature

$$T_{\text{die}} = T_{\text{ambient}} + \text{ThermalR}_{\text{Pkg}} * \text{Power}_{\text{Chip+I/O}}$$

- Using die temperature in SPICE

```
.TEMP 50
```

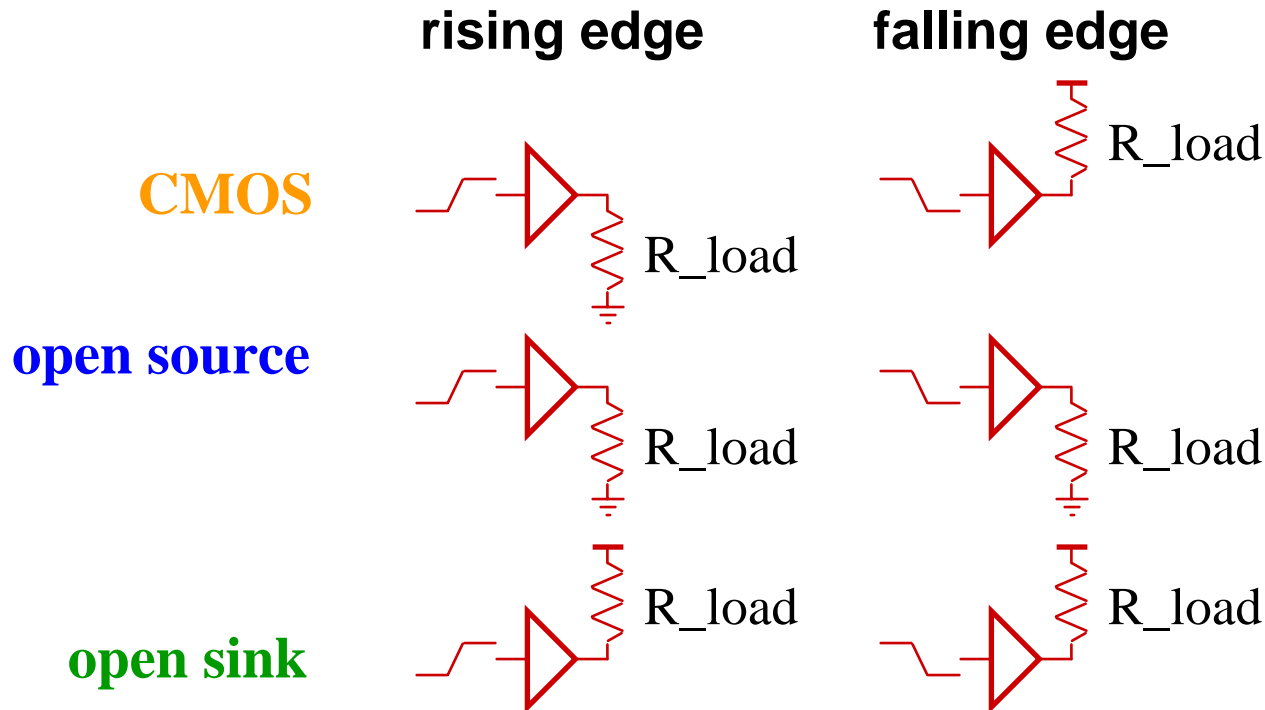
Model Creation

Obtaining parameters

- Interface specifications
 - Vinh, Vinl
 - Test loads
 - PCB trace impedances
 - Edge rates
- Could use these in SPICE
 - Simulations for C_comp

Model Creation

Obtaining [Ramp] parameters

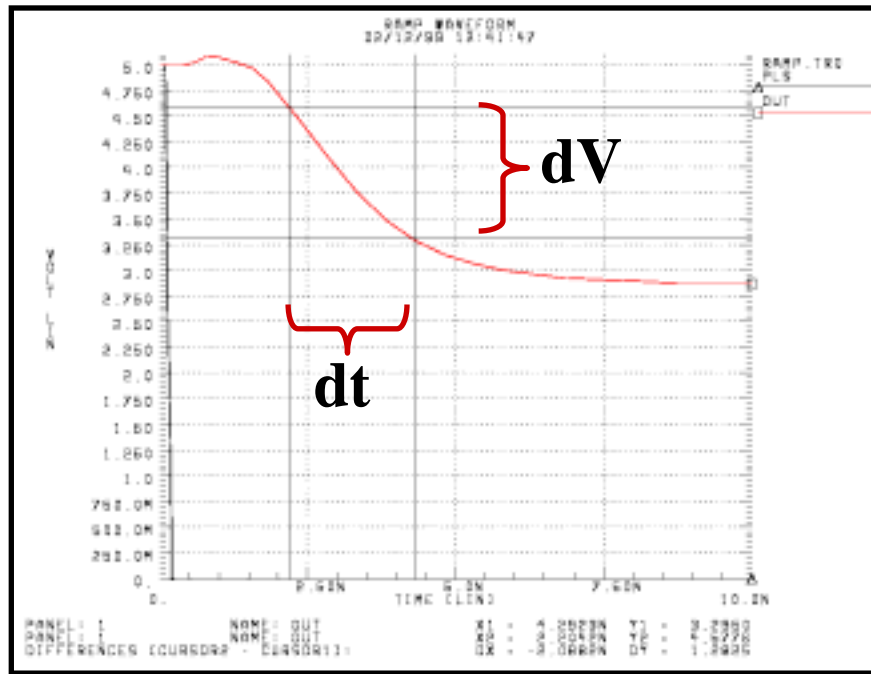


Make sure **R_load** is connected to the appropriate supply!

Model Creation

Obtaining [Ramp] parameters

- Find the 20 - 80 % points of the signal swing
- Read the voltage difference dV
- Read the time difference dt
- Enter those dV and dt values in [Ramp] format



Model Creation

Obtaining tables

- SPICE Simulations (or Test Bench Measurements)

$$T_{\text{die}} = T_{\text{ambient}} + \text{Thermal}R_{\text{Pkg}} * \text{Power}_{\text{Chip+I/O}}$$

- Dual-voltage I/O
 - Do Vcc_core and Vcc track?
- SPICE: 8-corner vs. 16-corner vs. 32-corner
 - Factor of 2 for each independent variable
 - Vcc, Temp, N_process, P_process, Vcc_core, ...
 - Which combinations are “min” and “max”?
- Use those “min” and “max” in Spice-to-IBIS

Model Creation



- IBIS File/Model tools
- IBIS parser (free download)
- HyperLynx Visual IBIS Editor
- s2ibis2 (open source, from NCSU)
- Cadence Model Integrity

Demo of Model Integrity to create buffer model and IBIS file

Obtaining Tables

Setting up SPICE

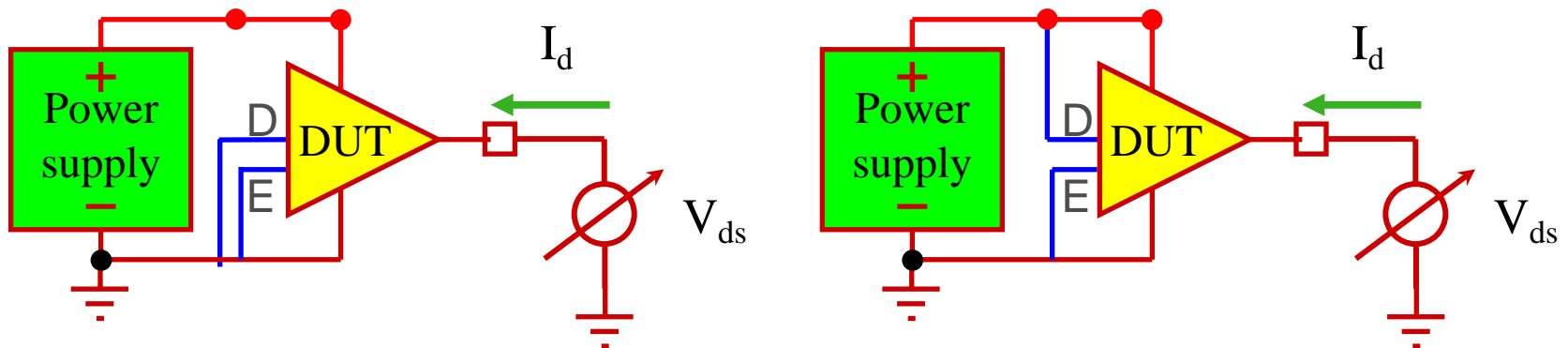
- Using template files or scripts
- Customizing
 - Temperature
 - Power supply voltage(s)
 - Number of pins on the buffer
 - Order of pins on the buffer
- Process model names
 - Using .MOD statements with the transistors
 - Diode models

Model Creation

Obtaining I-V tables

- No package when generating buffer tables
- Single-ended driver
- Sweep V_{ds} from $-V_{cc}$ to $+2V_{cc}$

Pulldown + GND clamp + Power Clamp Pullup + GND Clamp + Power clamp



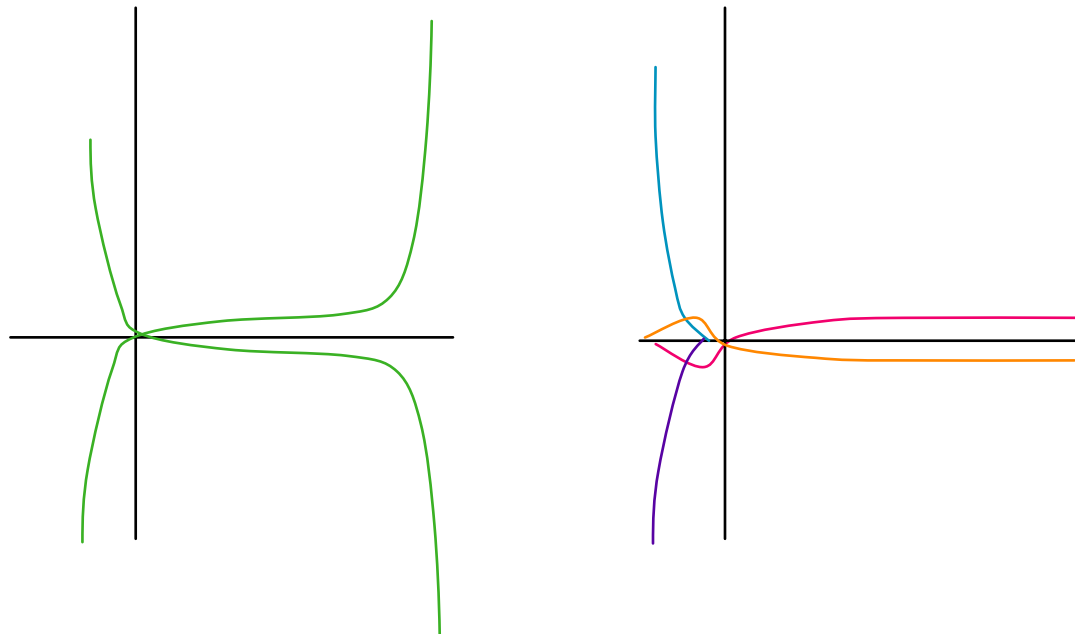
Note: Currents are considered positive when their direction is into the IBIS buffer or component.

Model Creation

Obtaining I-V tables

- Note: Don't forget the diode resistance (RS in SPICE)!
- Separate **total** currents into:

- Pulldown
- Pullup
- Power clamp
- GND clamp

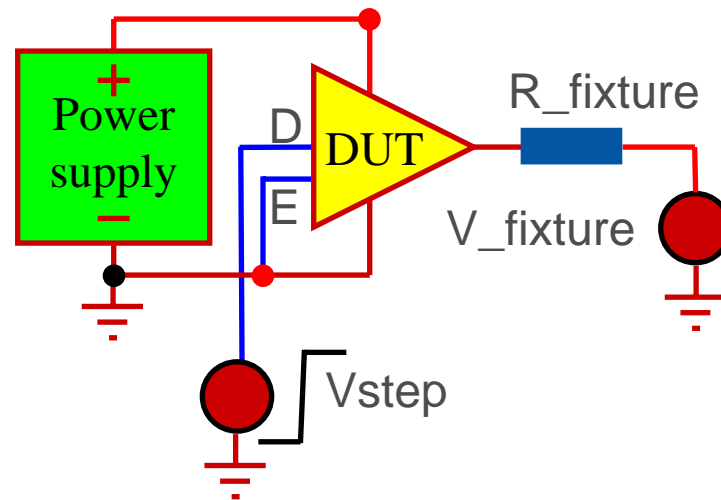


- Make Pullup and Power clamp Vcc-referenced

Model Creation

Obtaining V-t tables

- V_{step} at core edge rate
- Single-ended driver
- Four tables
 - $D=\text{Low}$, $V_{\text{fixture}}=0$
 - $D=\text{Low}$, $V_{\text{fixture}}=V_{\text{cc}}$
 - $D=\text{Hi}$, $V_{\text{fixture}}=0$
 - $D=\text{Hi}$, $V_{\text{fixture}}=V_{\text{cc}}$
- Can use sets of 4 tables
 - Different R_{fixture} for each set



Model Creation

Interpreting V-t tables

```
[Rising Waveform]
| Time          V(typ)
0.00s          25.21mV
0.20ns        35.33mV
```

```
[Falling Waveform]
| Time          V(typ)
0.00s          325.21mV
0.20ns        322.33mV
```

```
[Rising Waveform]
| Time          V(typ)
10.00s         25.21mV
10.20ns       35.33mV
[Falling Waveform]
| Time          V(typ)
10.00s         325.21mV
10.20ns       322.33mV
```

```
[Rising Waveform]
| Time          V(typ)
5.00s          25.21mV
5.20ns        35.33mV
[Falling Waveform]
| Time          V(typ)
10.00s         325.21mV
10.20ns       322.33mV
```

Model Creation

Interpreting V-t tables

- What about those “flat” times
- V-t is not changing, but table contains data
- Actual internal buffer delays
- Different tools do different things!

```
[Rising Waveform]
| Time          V(typ)
0.0ns          25.21mV
2.0ns          25.21mV
2.20ns         2.33mV
. . . .
5.00ns         0.034mV
20.00ns        0.034mV
```

Model Creation

Ways to Obtain C_comp

- Remember the goals
 - Signal integrity (reflections, crosstalk)
 - Timing (PCB delays)
- Things to include in C_comp
 - Metal capacitances
 - Silicon junction capacitances
- There is no one C_comp value!
 - Might want to manually adjust value

Model Creation

Ways to Obtain C_comp

- Time domain (large signal) effects
 - Edge rate
 - Voltage step values

Frequency (small signal) effects

- Frequency (small signal)
- DC bias voltage sensitivity
- As seen at die pad

Model Creation

Ways to Obtain C_comp

- Step response $I = C \, dV/dt$
 - Using PCB edge rates and voltages
- Tuned tank resonance $\omega = 1/\sqrt{C_{\text{comp}} * L_{\text{ext}}}$
 - Voltage sensitivity
 - Narrowband frequency sweep
- Zout pole frequency $\omega = 1/RC$
 - Single bias
 - Wideband frequency sweep

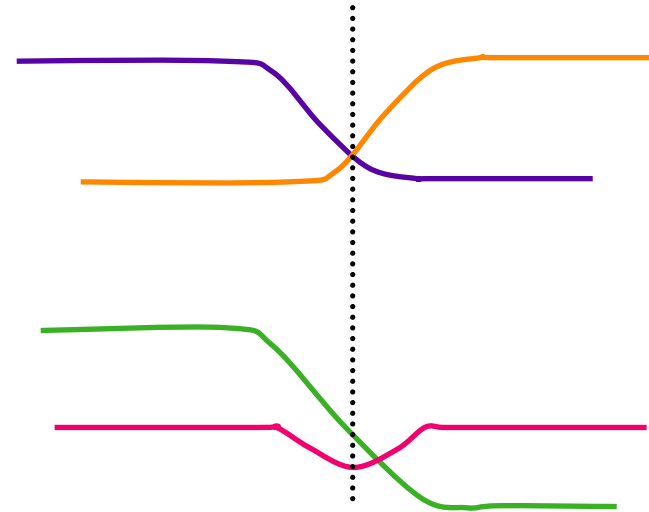
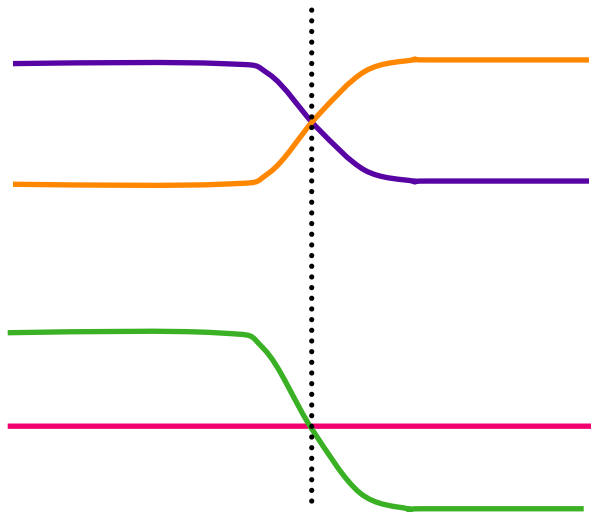
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- On-die Terminators
- LVDS Model Example
- High-Speed Interconnect Models

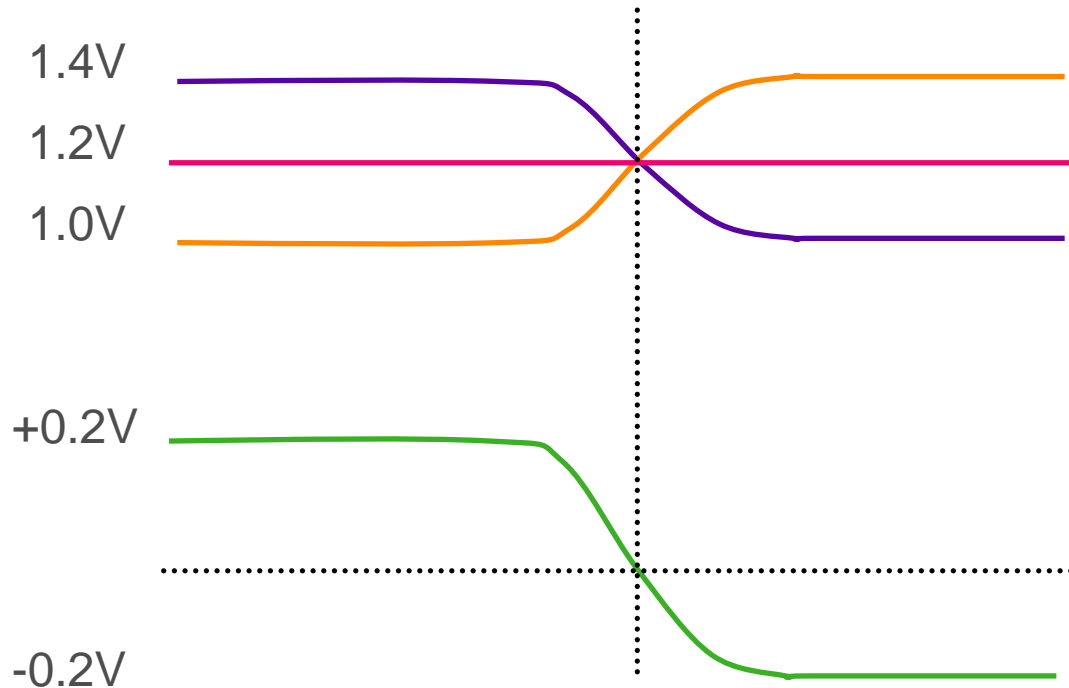
Differential Signals

- Non-inverting pin signal
- Inverting pin signal
- Differential signal
- Common mode signal



Differential Signals

- Ideal LVDS switching



Pseudo-Differential Signals



- Single Buffer
- Single trace to route
- Receiver referenced to Vext
- Sensitive to crosstalk
- Sensitive to bounce in Vext

Paired-differential Signals



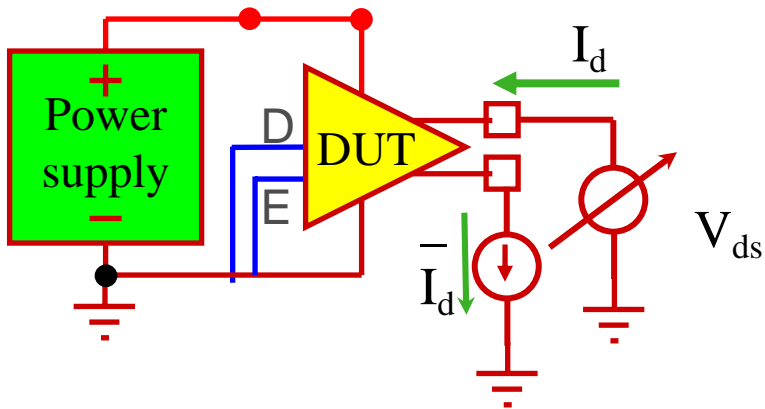
- Inverting and Non-inverting Buffers
- Data is inverted
- Independent circuits
- Independent currents
- Better than single-ended differential
 - Reduced crosstalk sensitivity
- Not as good as true differential
 - Slew rise/fall often not matched

Model Creation

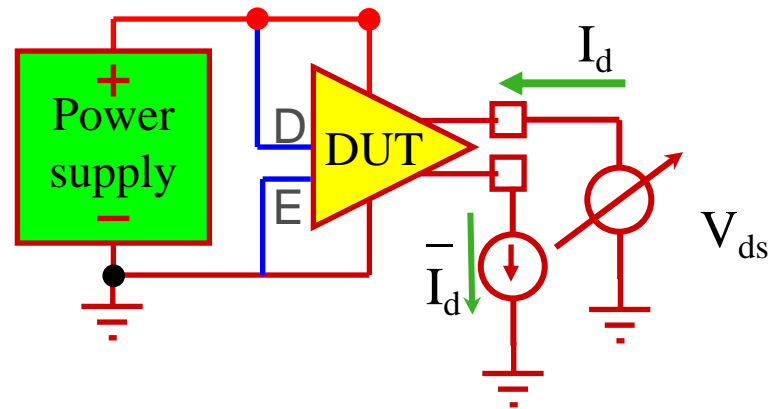
Differential I-V tables

- No package when generating buffer tables
- Differential driver
 - Complementary current

Pulldown + GND clamp + Power Clamp



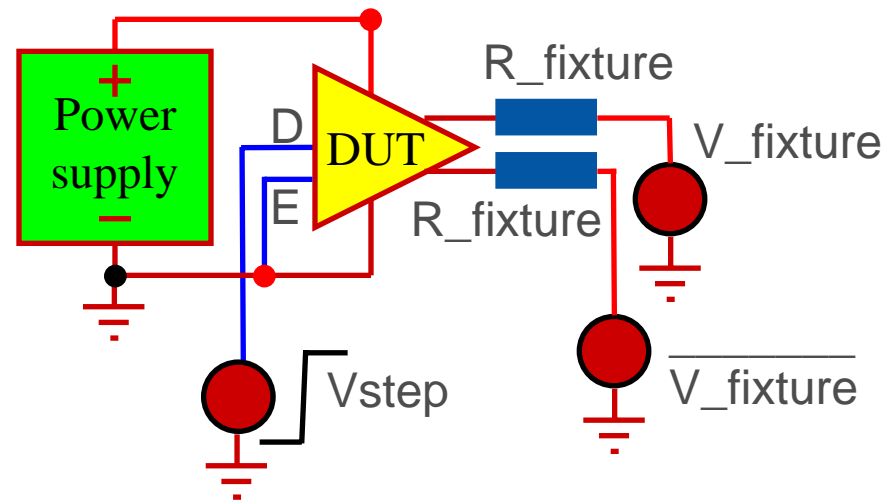
Pullup + GND Clamp + Power clamp



Model Creation

Obtaining V-t tables

- V_{step} at core edge rate
- Complementary voltage
- Without terminators
 - If represented separately
- Four tables
 - $D=\text{Low}$, $V_{\text{fixture}}=V_{\text{low}}$
 - $D=\text{Low}$, $V_{\text{fixture}}=V_{\text{high}}$
 - $D=\text{Hi}$, $V_{\text{fixture}}=V_{\text{low}}$
 - $D=\text{Hi}$, $V_{\text{fixture}}=V_{\text{high}}$



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- **Validation Methodology**
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IBIS Models In The Design Chain: What designers receive

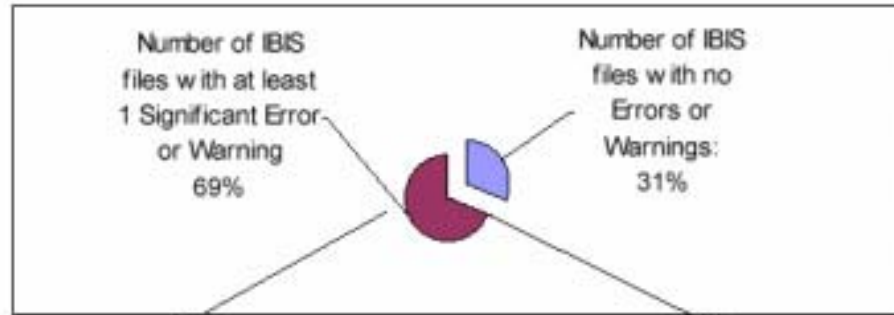
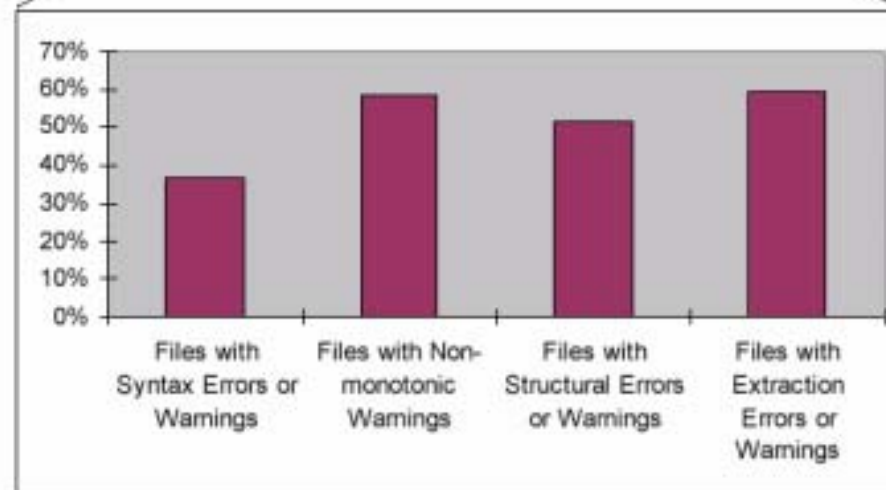


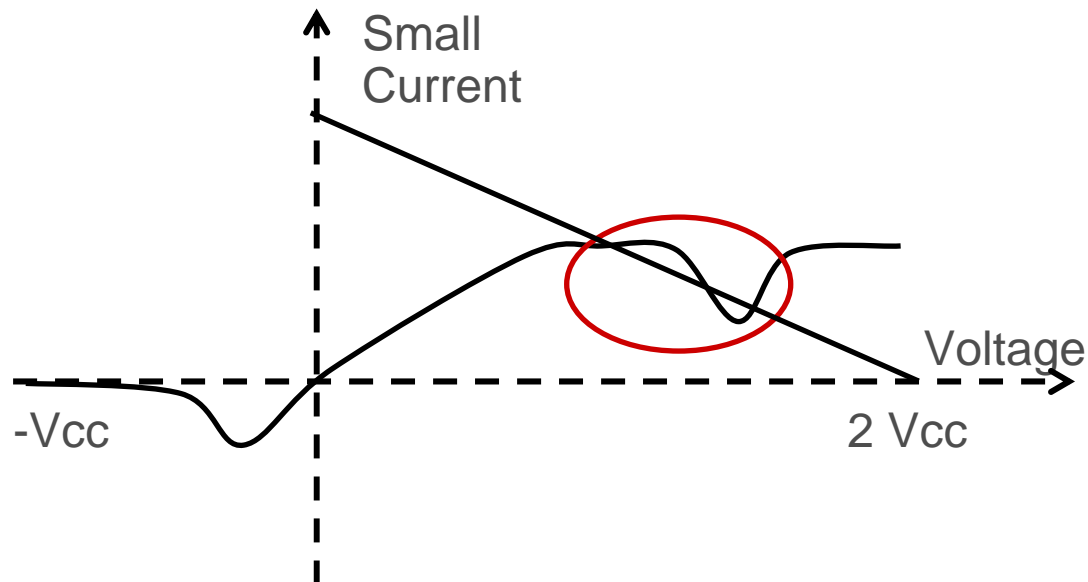
Figure 3-2: Ratio of Bad IBIS Files to Good IBIS files



“A Critique of IBIS Models Available for Download on the Web”, SiQual (IBIS Summit, 2002)

Pullup and Pulldown tables

- Non-monotonic driver characteristics (feedback)
- Potential for simulator convergence problems
- Most common buffer model issue



Addressing Common Problems

A Validation Methodology



- Validate
 - Each IBIS model
 - Completed IBIS file
- SPICE-to-IBIS tools
 - s2ibis2 has several known bugs
 - Most tools handle single-ended buffers
- IBIS spec lacks many “differential” features
 - IBIS 4.x will address these

Addressing Common Problems

A Validation Methodology

- Parse to check syntax (ibischk3)
- Examine parameters
- View tables graphically
- Other data checks
- Simulate
- Release for design use
- Close the loop

Addressing Common Problems

A Validation Methodology



- Recent IBIS model validation presentations

<http://www.cadencepcb.com/webinar/Modeling/frmModeling.asp>

<http://www.cadencepcb.com/webinar/Modeling2/frmModeling.asp>

- Other links with IBIS validation and model creation papers

<http://www.cadencepcb.com>

<http://www.eigroup.org/ibis/articles.htm>

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On-die Terminators



- High-speed differential termination
- Inside the package and bond wire
- Minimizes reflection effects at the receiver
- Fixed or variable resistance

Representing On-die Terminators

Many ways to do this

- Use “terminator” model type
- Use [Series Current]
- Use [Series MOSFET]
- Include current in one of the clamp tables
- Include in a SubModel
 - Termination can be disabled
 - Value can be changed

Representing On-die Terminators Tradeoffs



- Ease of model creation
- Linear or non-linear load
- Actual FET or pass-gate load
- Support in a specific simulator

Representing On-die Terminators

Terminator in buffer method

- Do this within the [Model]

- To insert a resistor to GND

variable	R(typ)	R(min)	R(max)
[Rgnd]	100ohm	80ohm	120ohm

- To insert a series resistor

variable	R(typ)	R(min)	R(max)
[R Series]	8ohm	6ohm	12ohm

Representing On-die Terminators

Series current between pins

- Define series connection for component

```
[Series Pin Mapping] pin_2 model_name function_table_group
4 5 Rser1 | Series Resistor, always ON
```

- Define (linear or non-linear) resistance using I-V table

```
[Series Current]
```

Voltage	I(typ)	I(min)	I(max)
-5.0V	-3900.0m	-3800.0m	-4000.0m
-0.7V	-80.0m	-75.0m	-85.0m
-0.6V	-22.0m	-20.0m	-25.0m
-0.5V	-2.4m	-2.0m	-2.9m
-0.4V	0.0m	0.0m	0.0m
5.0V	0.0m	0.0m	0.0m

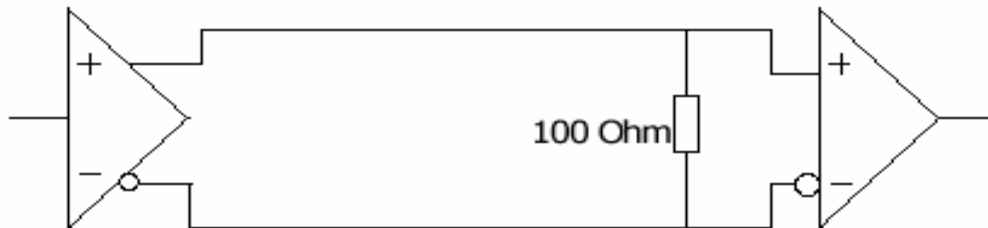
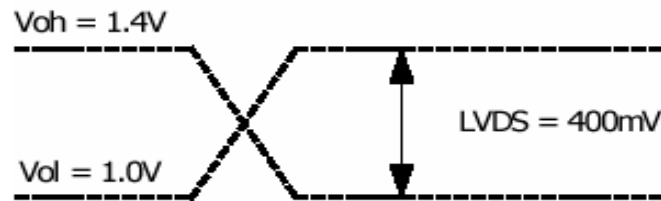
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- **LVDS Model Example**
- High-Speed Interconnect Models

LVDS Model Example

- Ideal LVDS operation
- 400 mV differential mode
- 1.2 V common mode
- 100 Ω termination



LVDS Model Example

V-t tables

- V-t tables needed for DC operating point
- Timing between rising and falling edges
- Timing relative to core data signal
- Examples

LVDS Model Example



- LVDS IBIS Models @ 1.25GHz
 - Douglas Burns, SiSoft
 - Used for next two slides
 - Intentional time offset in plots

IBIS Summit <http://www.eda.org/pub/ibis/summits/jun02>

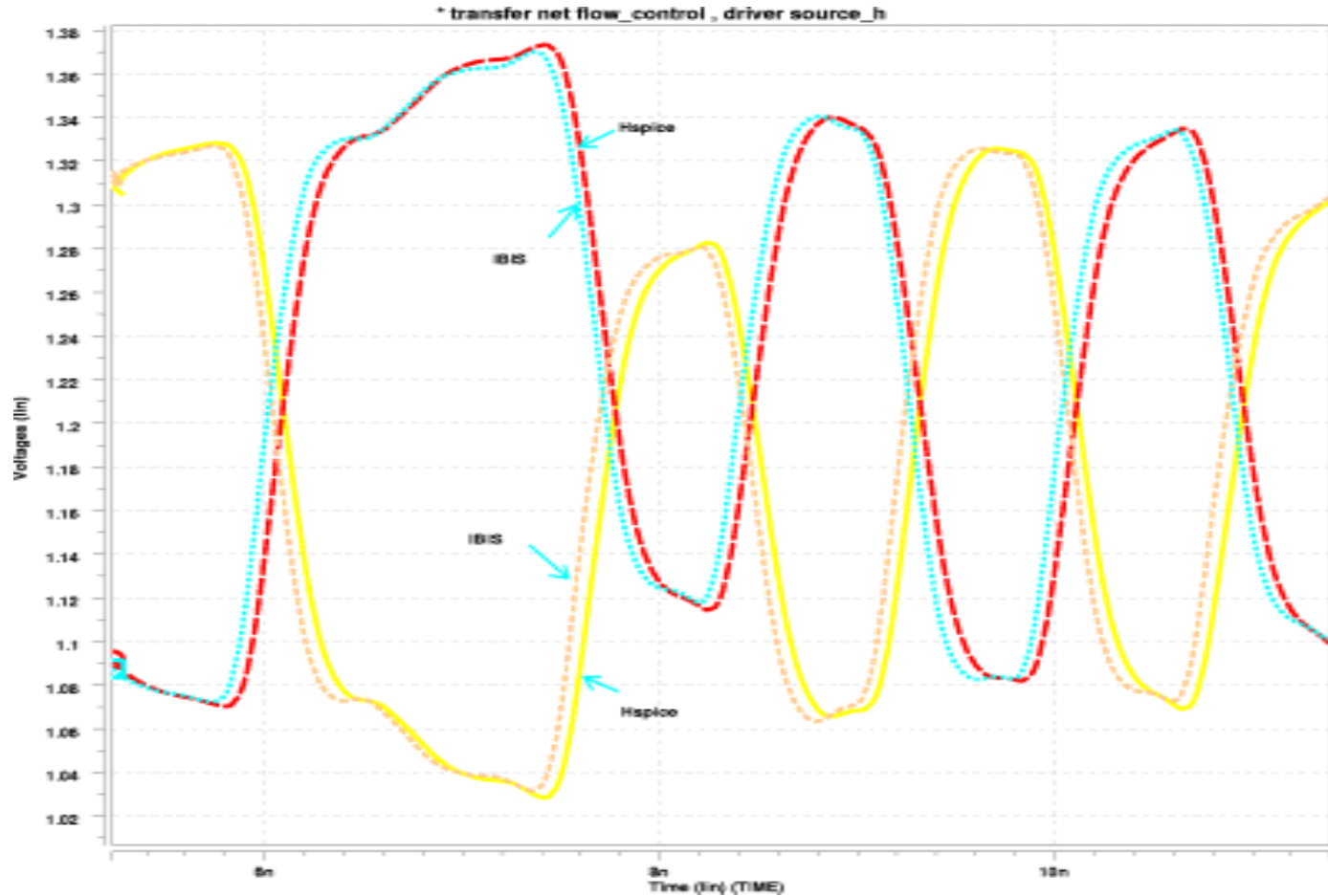
burns.zip: LVDS IBIS Models @ 1.25GHz (.ppt)

burns.pdf: Douglas Burns, Steven Coe, and Kevin Fisher,
Signal Integrity Software (SiSoft)

- Capabilities and limitations of IBIS models

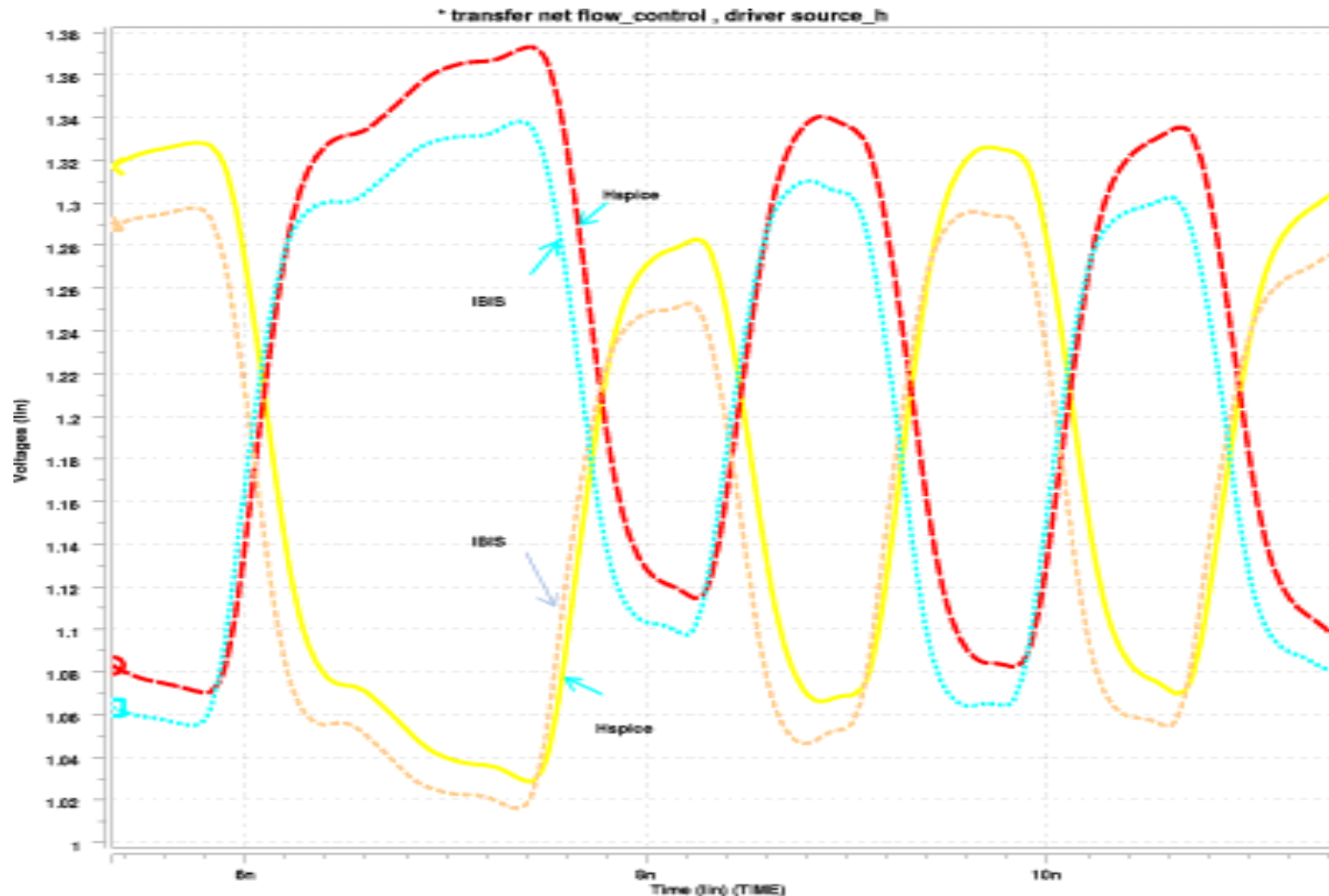
Accurate LVDS IBIS Model @ 1.25GHz

SiSoft presentation



SPI4 interface: 1.25GHz, target pad, VDDQ=2.375

Effects of Changing VDDQ SiSoft presentation



SPI4 interface: 1.25GHz, target pad, VDDQ=2.325,
Model generated w/VDDQ=2.375

LVDS Model Example



- Model made at one V_{common}
 - Not valid if V_{common} changes
- Implications
 - Hard to select Min, Max conditions
 - Submodels for different V_{common}
 - Changing V_{common} with bit pattern
- IBIS was never designed to handle this!

LVDS Model Example

The IBIS 4.x solution

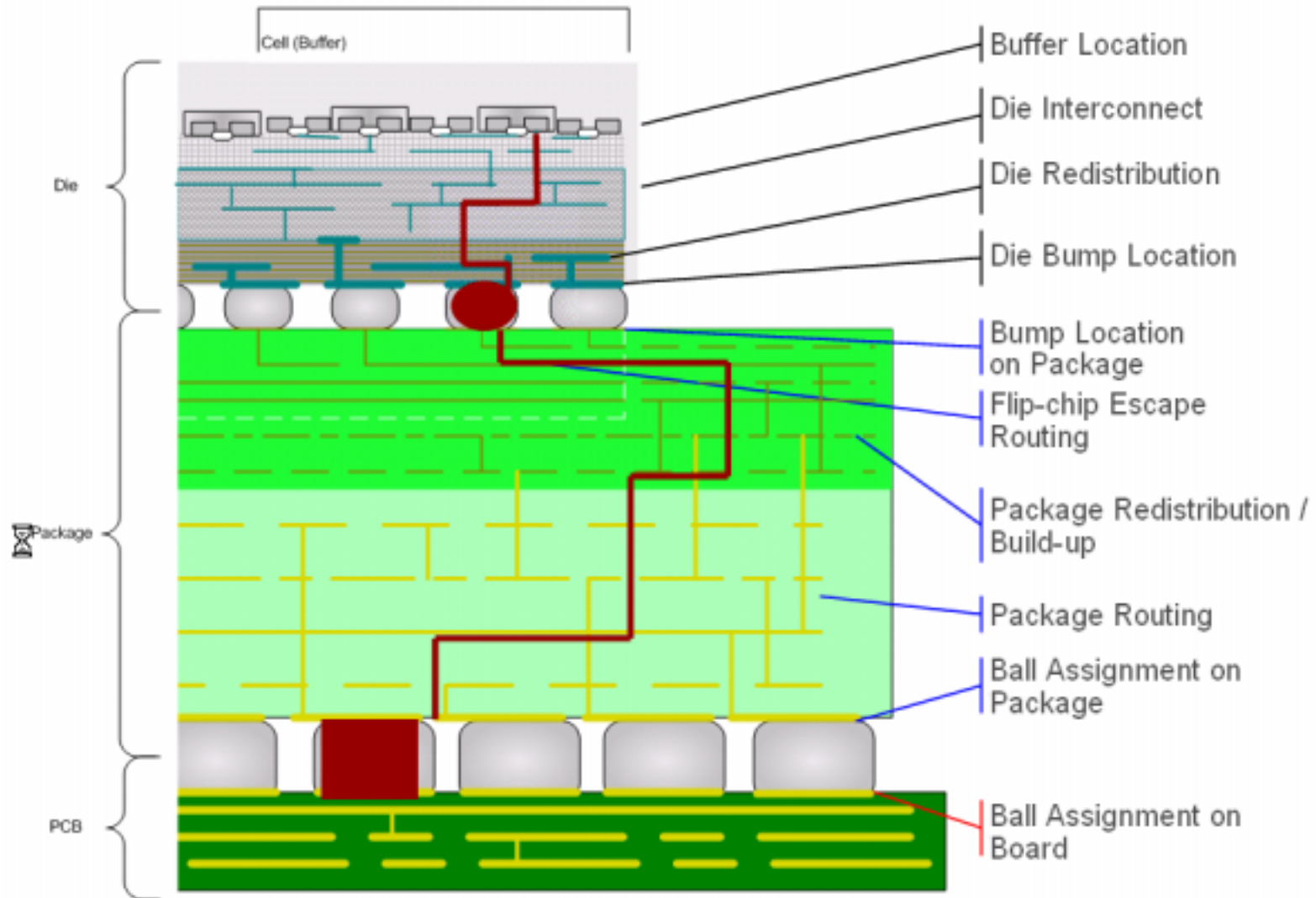
- IBIS 4.x approach
 - SPICE, Verilog-AMS, VHDL-AMS
- LVDS model in SPICE
 - Requires both circuit and process data
 - Multiple NDAs could be required
- LVDS models in an AMS language
 - Behavioral equations
 - Use of both digital and analog information
 - Including effects not addressed in IBIS 4.0

Overview



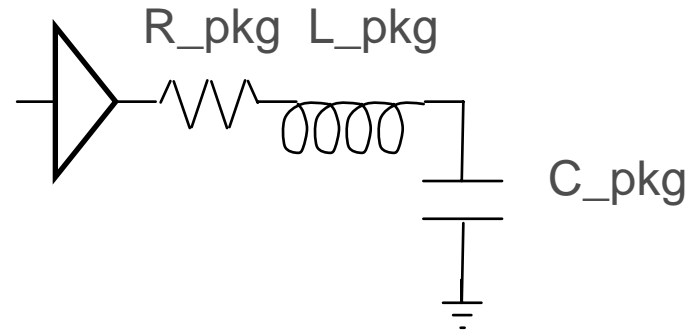
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High-Speed Interconnect Models



High-Speed Interconnect Models

- IBIS lumped package
 - R_{pkg} , L_{pkg} , C_{pkg}
 - Parameters are required
 - Values can be 0.0
 - Can define Typ/Min/Max values
- Packages are transmission lines
 - Impedance
 - Delay



High-Speed Interconnect Models



- Lumped parameters
 - Only valid at slow edge rates
 - Do not represent impedance changes
- Use of default parameters
 - Can set on a pin-by-pin basis

[Pin]

! Pin name	Model Name	R_pkg	L_pkg	C_pkg
D1	IO_1			
DD1	IO_1	0.090	6n	7p
DD2	IO_1	0.120	10n	12p

High-Speed Interconnect Models



- Lumped vs. distributed parameters
 - Could result in different values
- Distributed parameters
 - Should not use lumped parameters
 - Use EBD or (coupled) Package or Interconnect
 - Valid at both fast and slow edge rates

High-Speed Interconnect Models



- Characteristics of high-speed packages
 - Lumped model is not adequate
 - Signal and signal-power/gnd trace coupling
- EBD models for packages
 - Does not model any coupling
- PKG models for packages
 - Transmission line models
 - RLC matrices for coupling
- Interconnect models for packages (draft)
 - Touchstone S-parameter support

High-Speed Interconnect Models

EBD example



```
[Path Description] IN0
Pin 1 | Edge of Module
Len=0 L=0.2n R=10m / | Lumped Connector trace
Len=2.1 L=2.0n C=12.0p / | Units in inches
Fork | A Tee-connection
Len=40 L=0.15n C=1.2p / | Units in mils
  Len=0 L=0.6 R=0.02 / | Bond wire to U0 Pin2
  Node U0.2
Endfork
  Len = 0 C = 0.8p / | Socket to U1 Pin2
  Len = 0 L = 3.7n / |
  Len = 0 R = 90m / |
Node U1.2
```

High-Speed Interconnect Models

EBD example



[Path Description] IN2

Pin 2

Len = 1.5 L=6.0n C=2.0p /	Trace on module
Len = 0 R=50 /	Series terminator
Len = 0.25 L=6.0n C=2.0p /	Trace between R and package
Node R2.1	Series resistor pack
Node R2.2	
Len = 0.25 L=6.0n C=2.0p /	Trace between R and package
Node U0.4	

[Reference Designator Map]

Ref Des	File name	Component name
U0	good1.ibs	nonesuch
U1	good1.ibs	nonesuch
R2	r10k.ibs	A_10K_Pullup

High-Speed Interconnect Models

PKG example



```
[Inductance Matrix]      Full_matrix
[Row]    1
3.04859e-07  4.73185e-08  1.3428e-08  6.12191e-09
1.74022e-07  7.35469e-08  2.7321e-08  1.33807e-08
[Row]    2
3.04859e-07  4.73185e-08  1.3428e-08  7.35469e-08
1.74022e-07  7.35469e-08  2.7320e-08  1.74022e-07
[Capacitance Matrix]    Sparse_matrix
[Row]    1
1          2.48227e-10
2          -1.56651e-11
[Row]    2
2          2.51798e-10
```

Summary



- Creating a high-speed model is non-trivial
- More than one way to do things
 - On-die termination
 - LVDS simulation
- True differential drivers are hard to model
 - IBIS assumes no signal coupling between buffers
 - IBIS Multi-Lingual approach (IBIS 4.x)

Acknowledgements



- IBIS training materials
 - Arpad Muranyi, Intel Corp.
- IBIS Summit Presenters
 - Luca Giacotto, Ecole Doctorale EEATS
 - Arpad Muranyi, Intel
 - Jim Bell, SiQual
 - Barry Katz and Doug Burns, SiSoft

- IBIS Web Site

- Home Page <http://www.eigroup.org/ibis/ibis.htm>
- Specifications <http://www.eigroup.org/ibis/specs.htm>

Also Cookbook and BIRDS

- Parser <http://www.eda.org/pub/ibis/ibischk3/>
- IBIS Summit papers <http://www.eigroup.org/ibis/articles.htm>
Also Training Materials
- Quality Checklist (draft) <http://www.sisoft.com/ibis-quality/checklist/>

- FREE Model Review Service

Email Reflectors



- ibis-users and ibis

ibis-request@eda.org

- SI-list

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