An Introduction to IBIS Models and Model Validation

Dr. Lynne Green

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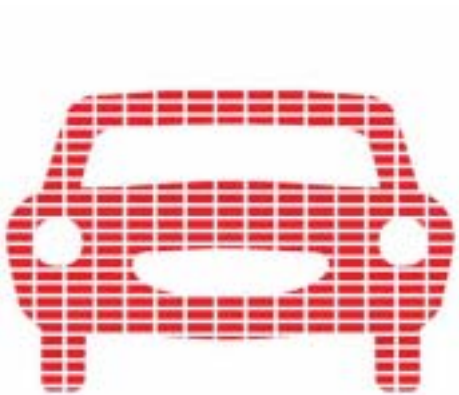
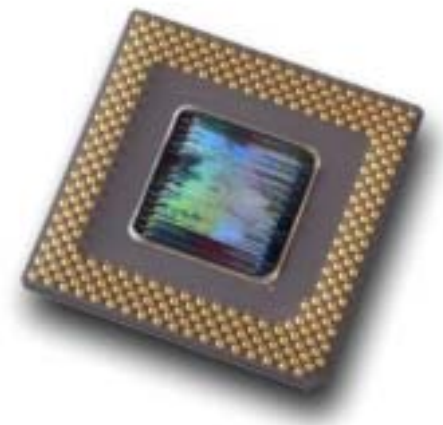
Overview

- IBIS Specification
- IBIS File Structure
- IBIS Component
- IBIS Models
- Interconnect Models
- IBIS Model Creation
- Validation Methodology
- Identifying Problems and Solutions

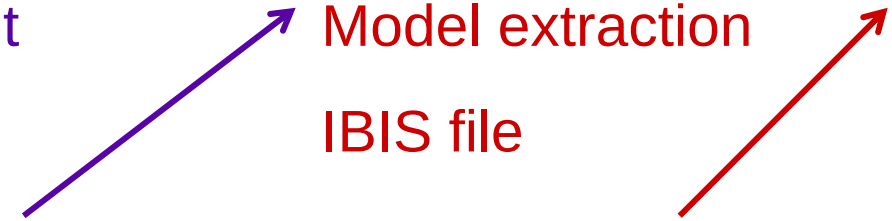
Overview
Levels of abstraction and detail





IBIS Models In The Design Chain

I/O Designer	Model Maker	PCB/SI Engineer
Circuit design	Simulation	PCB design
Cell layout	Model extraction	SI simulation
I/O netlist	IBIS file	Product



IBIS: I/O Buffer Interface Specification

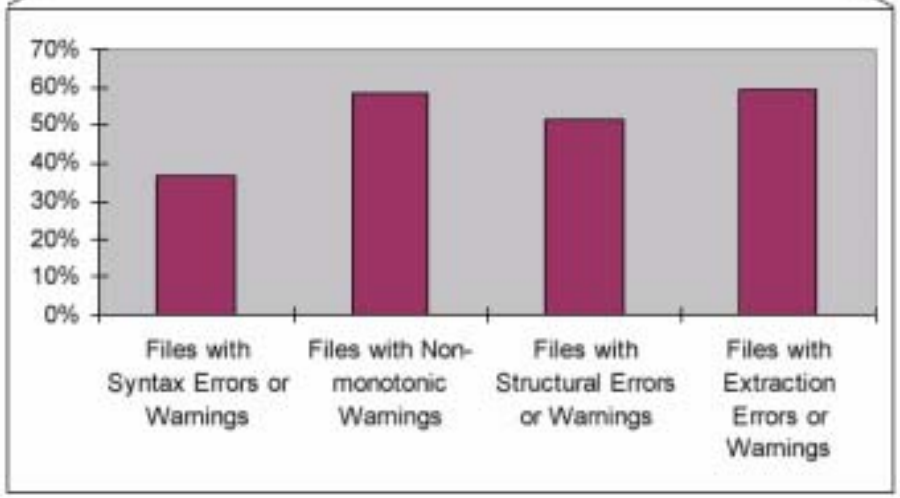
- Support fast signal integrity simulation
  - Reflections and delays
  - Overshoot and ringing
- Provide for portable model data
  - I/O buffers, series elements, terminators
  - SPICE “process” models are not portable
- Protect intellectual property
  - Protect circuit and process IP
  - Models can be built from test-bench data

EIA/ANSI 656-A
I/O Buffer Interface Specification

- Version 1.0 in 1993
  - Intel, Cadence Design Systems, Mentor Graphics, HyperLynx
- Version 4.0 in 2002
  - About 30 member companies (Model makers, models users, EDA)
- Version 4.1 in development
  - Add support for SPICE and AMS models
- Interconnect spec in development
- Publicly available parser
  - IBIS 3.2.9 parser today
  - IBIS 4.0 parser Q2/2003

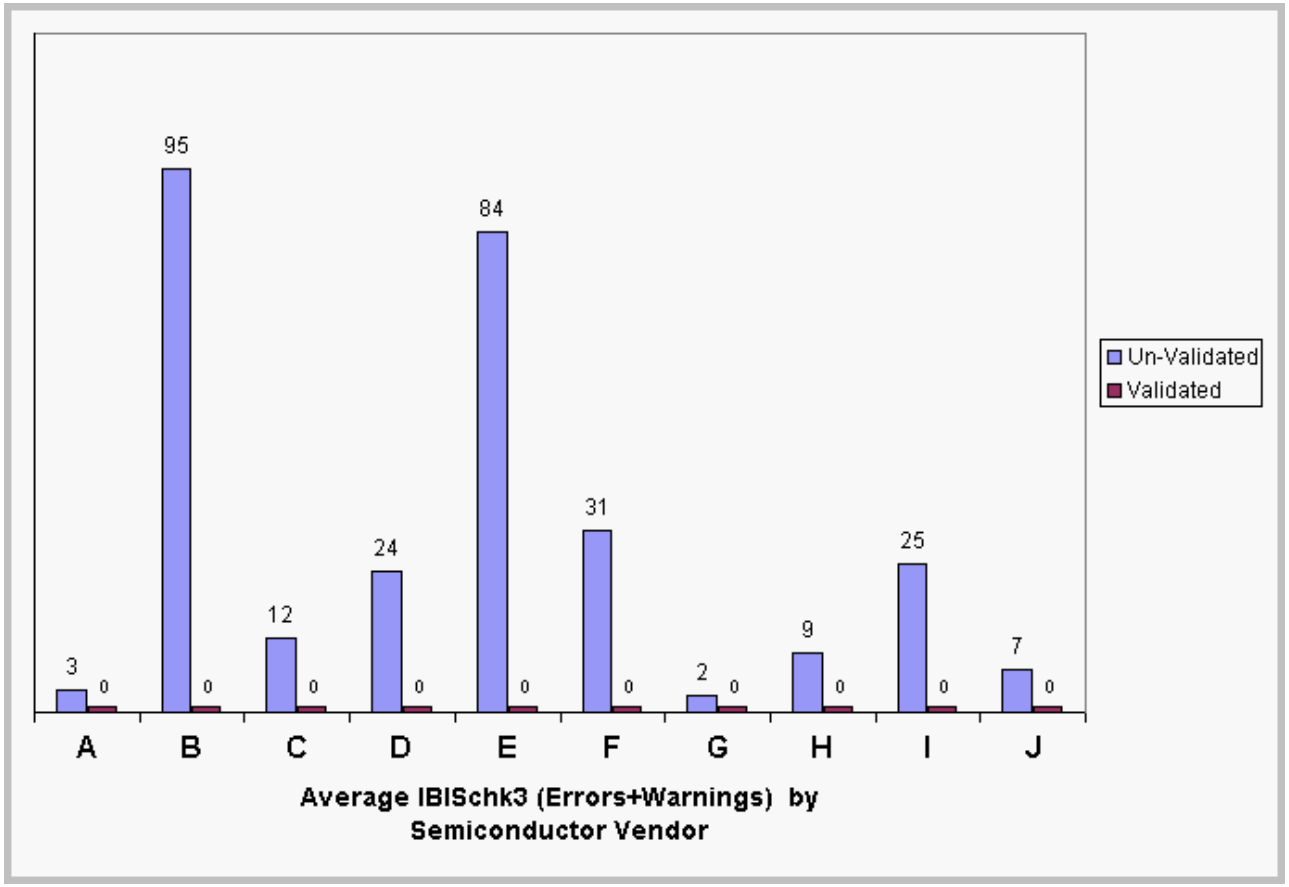
IBIS Models In The Design Chain: What designers receive

Figure 3-2: Ratio of Bad IBIS Files to Good IBIS files



"A Critique of IBIS Models Available for Download on the Web", SiQual (IBIS Summit, 2002)

Models In The Design Chain: What model makers provide



"IBIS Quality Committee Report", Barry Katz, Signal Integrity Software, Inc. (IBIS Summit 2002)

Creating IBIS Models

- Text editors (cut/paste, data columns)
- Scripts (customized flow)
- s2ibis2 (with modifications)
- Model Integrity

Buffer model and IBIS file flow (Demo)

The IBIS Specification

- Syntax
  - Keywords, sub-parameters, tables
- Data interpretation
  - I-V tables for pullup and pulldown
  - I-V tables for power and ground clamps
  - V-t tables
- Typ/Min/Max ordering
  - Different from datasheets
  - Package: use Typ, Min value, Max value
  - Models: use Typ, Slow/Weak, Strong/Fast

The IBIS Specification
Typ, Min, Max

- Min Corner
  - Weakest current
  - Slowest edge rates
  - Lowest voltage
- Typ Corner
  - Nominal
- Max Corner
  - Strongest current
  - Fastest edge rates
  - Highest voltage

The IBIS Specification
Typ, Min, Max

- Typ = Nominal voltage, temperature, process
- CMOS
  - Min @ minimum voltage, maximum temperature, and slow process
  - Max @ maximum voltage, minimum temperature, and fast process
- Bipolar
  - Min @ minimum voltage, minimum temperature, and slow process
  - Max @ maximum voltage, maximum temperature, and fast process

Note: Temperature is die temperature, not ambient.
Important in setting up SPICE simulations.

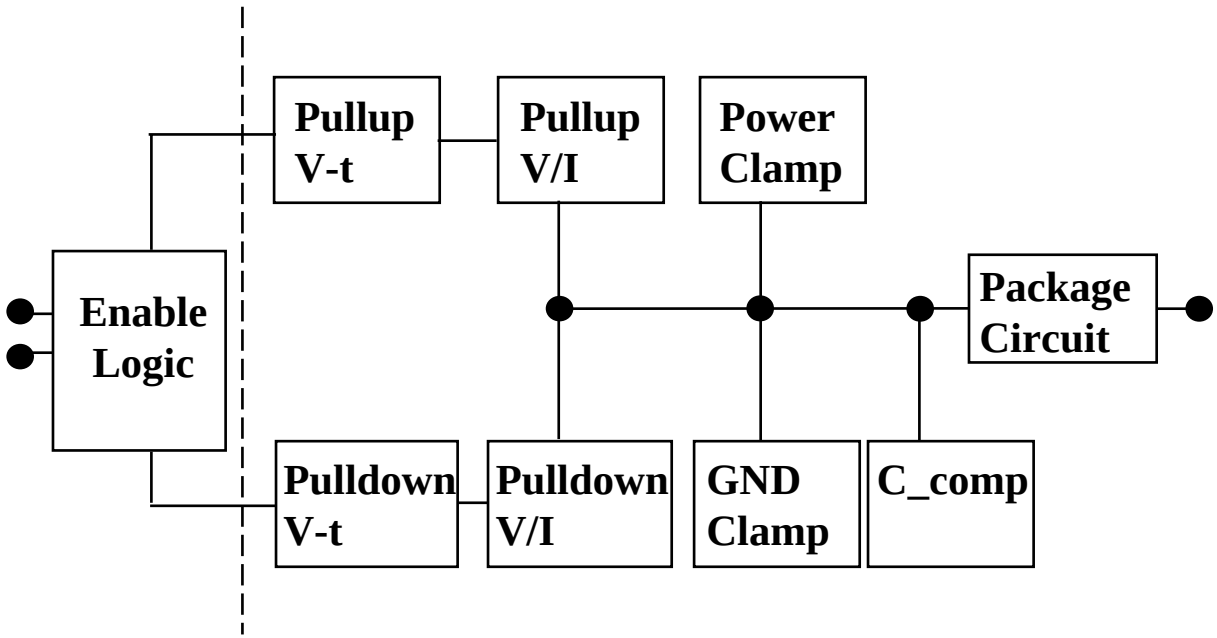
IBIS Syntax

- Keywords
  - Enclosed in [ ]
  - Use “ ” or “_”
  - Case insensitive
- Sub-parameters
- Names
  - Components, pins
  - Signals, models
  - Layout tool naming
- Comment Characters

```
[Component]      XYZ
[Manufacturer]   Nonesuch
[Package]
| variable    typ      min      max
R_pkg         0.10     0.05     NA
L_pkg         1.80nH   1.0n     3n
C_pkg         0.50pF   NA       NA
[Pin]
|pin_name    signal_name  model_name
1            trans1       demo1
B2           GND          GND
C1           VCC1         POWER
D2           N1           NC
```

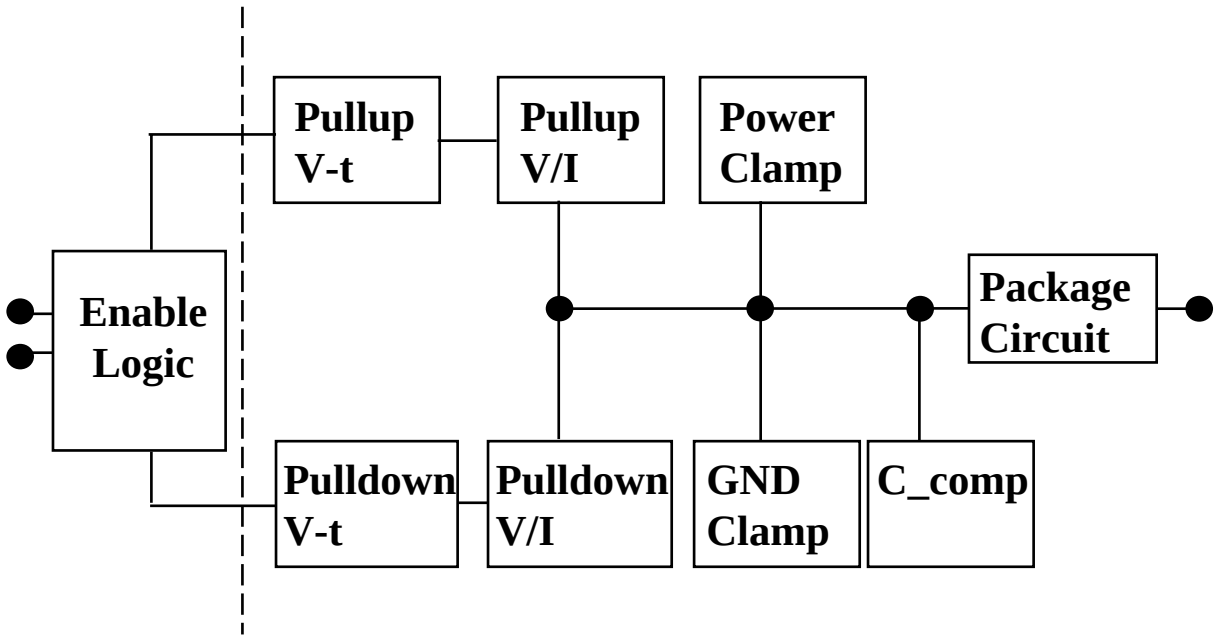
IBIS Data Interpretation

- I_dn = [GND clamp] + [Power clamp] + [Pulldown]
- I_up = [GND clamp] + [Power clamp] + [Pullup]
- I_rcvr = [GND clamp] + [Power clamp]



IBIS Data Interpretation

- Output transitions
- V-t tables preferred
- [Ramp] values are also used



IBIS Data Interpretation

- Output transitions
- Multiple V-t tables
- Effect of load impedance

http://www.ntu.edu.sg/home/ehntan/glsvlsi.zip

http://www.sigrity.com/papers/ectc96/DOectc96ibis.htm

IBIS File Structure

- Header
- Comments
- Component data
  - One or more components
  - Pin, signal, model, package
  - Diff pin pairs, etc.
- Model data
  - One or more models

IBIS File Structure Header

- IBIS version
  - Highest version supported
  - First keyword in file
- File properties
- Date and file revision
- Legal disclaimer
- Copyright
- Documentation

```
[IBIS Ver] 3.2
[File Name] good1.ibs
[File Rev] 0.0
[Date] April 1, 1900
[Source] dummy data
[Notes] This model does not
represent any part from any
vendor.
[Disclaimer] Demo model, not
intended for design or system
simulation.
[Copyright] Cadence Design Systems
```

IBIS File Structure Header

- Disclaimer
  - Similar to what appears on the datasheet
  - Model is not guaranteed for any specific use ...
  - Subject to change without notice ...
- File revision
  - 0.x: silicon and file in development
  - 1.x: pre-silicon file data from silicon model only
  - 2.x: file correlated to actual silicon measurements
  - 3.x: mature product, no more changes likely

IBIS File Structure Components

- [Component]
  - Can have more than one per file
- [Manufacturer]
- [Package]
- [Pin]
  - Every pin on physical package
  - Optional package parasitics
  - Case-sensitive
  - Match pin case to layout

```
[Component]      nonesuch
[Manufacturer]   nobody
|
[Package]
| variable typ     min    max
R_pkg       100m    NA     NA
L_pkg       6nH     NA     NA
C_pkg       1.5pF   NA     NA
|
[Pin] signal_name   model_name
1      io1          demo1
2      io2          demo1
B2     Vcc1         POWER
C3     Gnd1         GND
A10    unused       NC
```

IBIS File Structure Components

- [Diff Pin] pairs

```
[Diff Pin] inv_pin vdiff tdelay_typ tdelay_min tdelay_max
1          2       0.15V  -1ns       0ns         -2ns
```

- [Series Pin Mapping] pairs

```
[Series Pin Mapping] pin_2 model_name function_table_group
1                    2     CBTSeries  1
[Series Switch Groups]
| Function Group States
On 1 2 /
```

- [Model Selector]

```
[Model Selector] Progbuffer1
OUT_2            2 mA buffer without slew rate control
OUT_4S           4 mA buffer with slew rate control
```

IBIS File Structure
I/O Buffer Models

- Model used by one or more pins
- May be used by more than one component
- Model name is unique within the IBIS file
- 17 pre-defined model types
  - Input, Output, I/O, 3-state
  - Open_sink, I/O_open_sink, Open_source, I/O_open_source
  - Input_ECL, Output_ECL, I/O_ECL, 3-state_ECL
  - Series, Series_switch
  - Terminator
  - Open_drain and I/O_open_drain obsolete

IBIS File Structure
I/O Buffer Models

- Model header
- Voltage keyword(s)
- Input values
  - Logic levels
- Output values
  - Polarity
  - Enable
  - Standard load
  - Ramp

```
[Model]     demo1
Model_type   I/O
Polarity        Non-Inverting
Enable          Active-High
Vinl = 1.3
Vinh = 1.7
Cref = 10p
Vmeas = 1.5
| variable                  typ   min   max
C_comp                      3pF   NA    NA
[Temperature Range]         50    125   0
[Voltage Range]             3.3   3.0   3.6
|[Pullup Reference]         3.3   3.0   3.6
|[Pulldown Reference]       0.0   0.0   0.0
|[POWER Clamp Reference]    3.3   3.0   3.6
|[GND Clamp Reference]      0.0   0.0   0.0
[Ramp]
dV/dt_r  1.20/0.9n 0.96/1.5n 1.46/0.7n
dV/dt_f  1.60/0.9n 1.38/1.4n 1.78/0.7n
R_load = 75ohms
```

IBIS File Structure
I/O Buffer Models

	Power_ Clamp	GND_ Clamp	Pullup	Pulldown	Vinh, Vinl	Vmeas
Input	Opt*	Opt*	No	No	Req	No
Output	Opt	Opt	Req	Req	No	Opt!
I/O	Opt*	Opt*	Req	Req	Req	Opt!
3–State	Opt*	Opt*	Req	Req	Opt	Opt!
Open_Sink	Opt*	Opt*	No	Req	No	Opt!
I/O_Open_ Sink	Opt*	Opt*	No	Req	Req	Opt!
Open_ Source	Opt*	Opt*	Req	No	No	Opt!
IO_Open_ Source	Opt*	Opt*	Req	No	Req	Opt!

* Should not be omitted unless the corresponding input clamping and leakage currents are 0 Amp.

! Required for timing checks.

IBIS File Structure
I/O Buffer Models

- I-V tables
  - [Pullup]
  - [Pulldown]
  - [Power Clamp]
  - [GND Clamp]
- Column ordering
- Monotonicity

```
[Pulldown]
| voltage I(typ)   I(min)   I(max)
-3.6      -1.1e-1  -8.0e-2  -1.3e-1
-1.0      -7.3e-2  -5.1e-2  -7.8e-2
-0.4      -3.6e-2  -2.9e-2  -4.1e-2
-0.1      -9.3e-3  -7.6e-3  -1.0e-2
0.0       0.0      0.0      0.0
0.1       9.2e-3   7.5e-3   1.0e-2
0.6       5.1e-2   4.0e-2   5.7e-2
1.0       7.8e-2   6.1e-2   8.9e-2
2.0       1.1e-1   8.4e-2   1.4e-1
2.5       1.2e-1   8.5e-2   1.5e-1
3.0       1.2e-1   8.6e-2   1.5e-1
3.3       1.2e-1   8.7e-2   1.5e-1
3.6       1.2e-1   8.7e-2   1.5e-1
6.6       1.2e-1   8.7e-2   1.5e-1
```

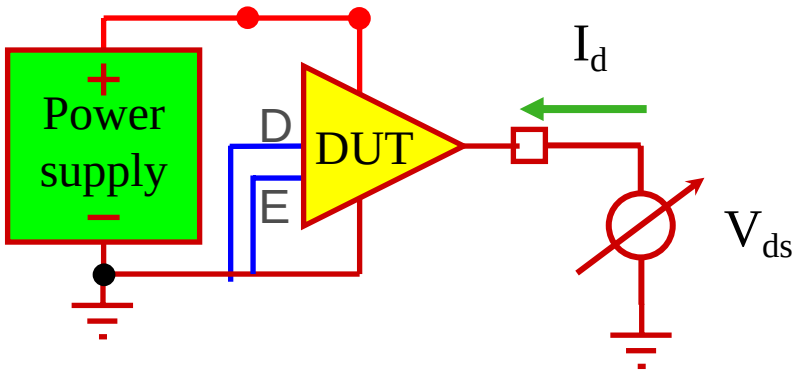
IBIS File Structure
I/O Buffer Models

- Monotonicity
  - Total current
- Simulator convergence
  - 0A at 0V
  - Final slopes
  - Best points selection
- Physical operation
  - Feedback effects
  - Over clocking

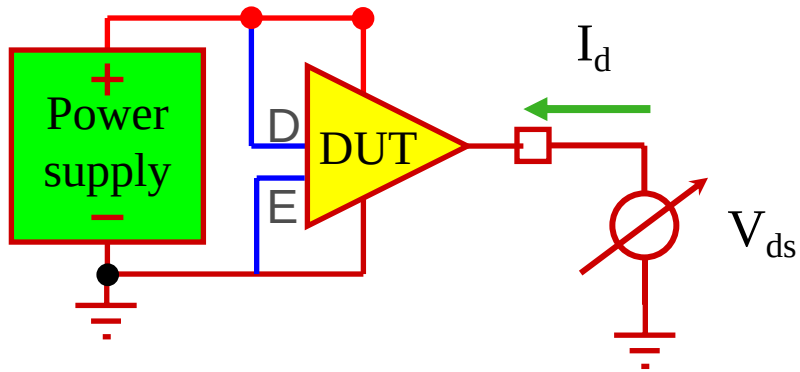
Generating Table Data

- I-V tables
  - Range is –Vcc to +2Vcc
  - Setting DC voltages (Typ/Min/Max)

Pulldown + GND clamp



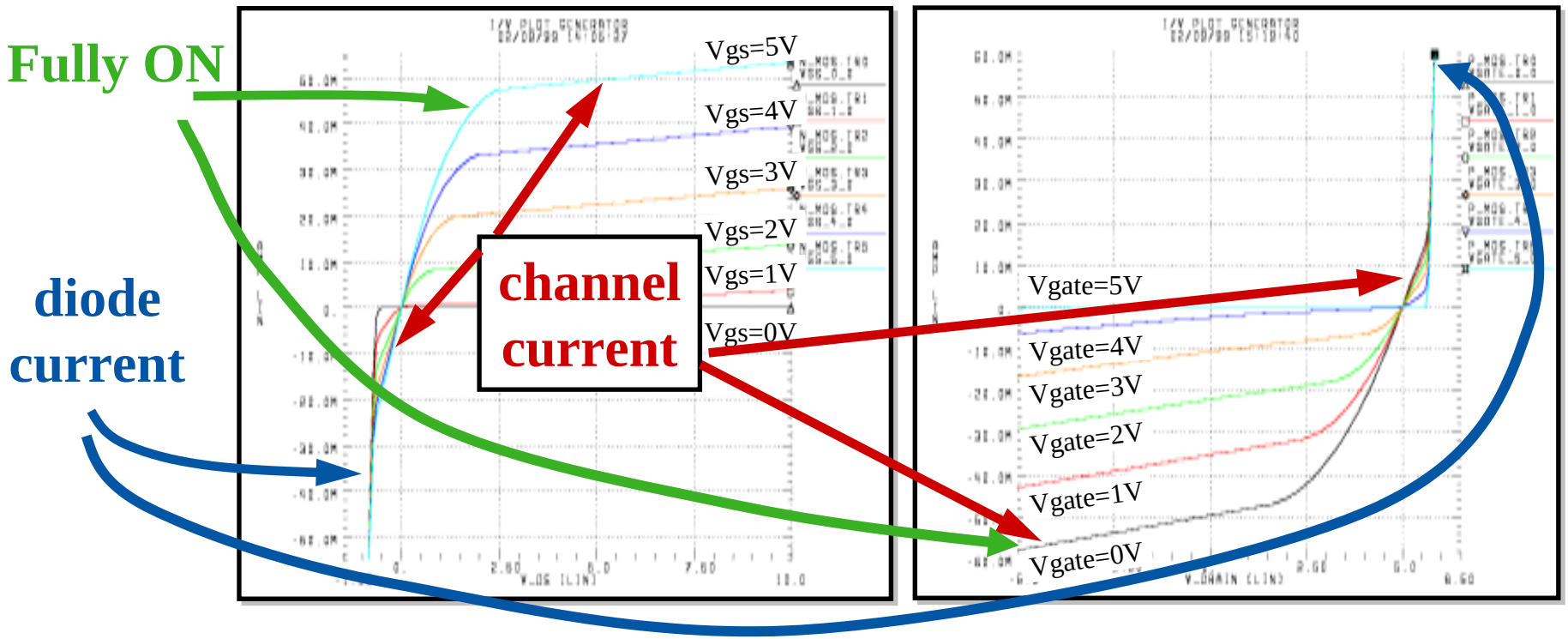
Pullup + Power clamp



Note: Currents are considered positive when their direction is into the component.

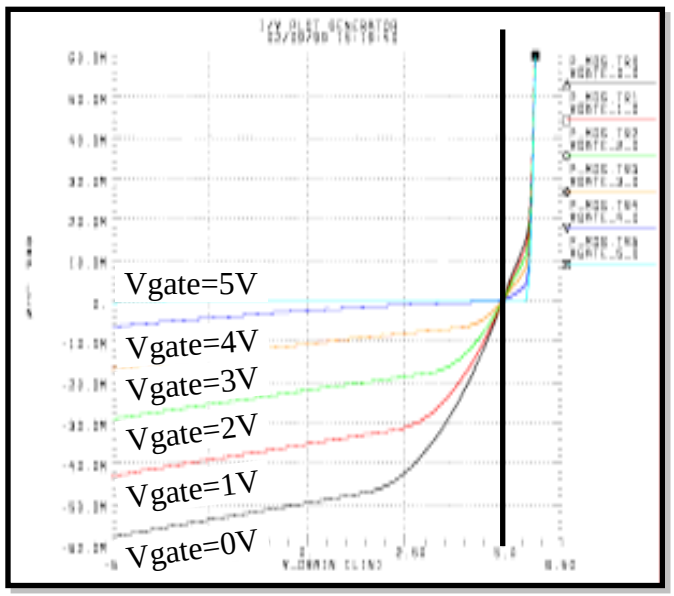
Generating Table Data

- Separating the drive and clamp currents

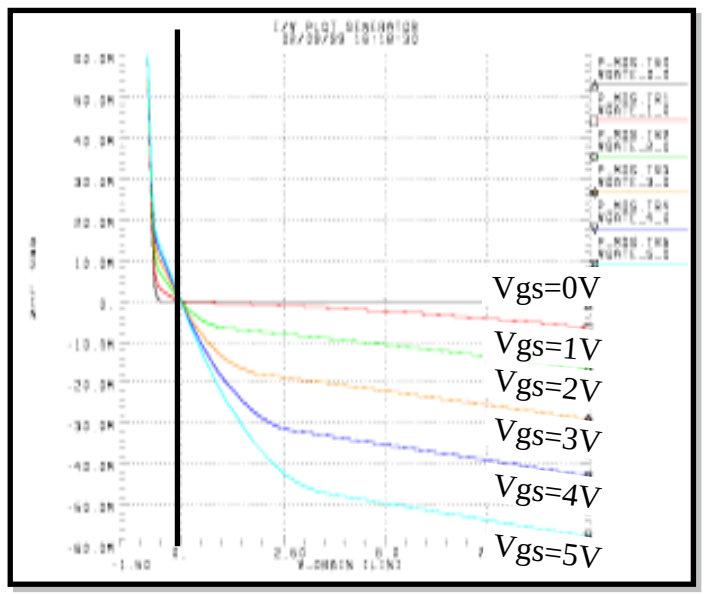


Generating Table Data
Extracting I-V tables

- I-V table
- Separating into Clamps and Drive tables
- Changing reference for Pullup and Power clamp tables



Vout



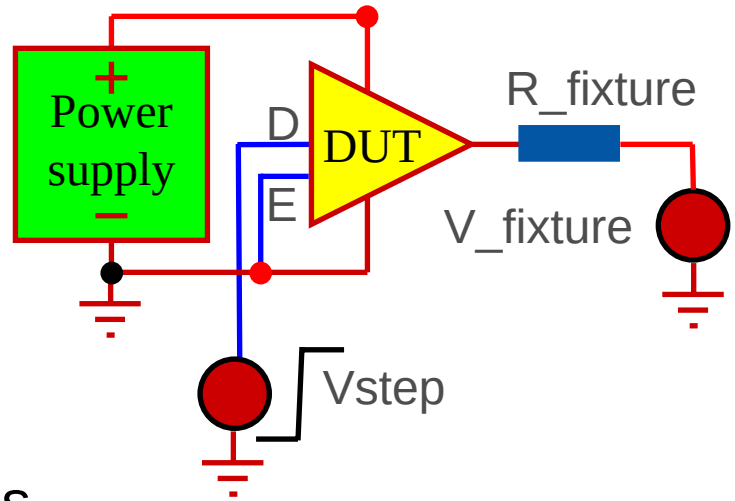
Vtable = Vcc-Vout

Generating Table Data

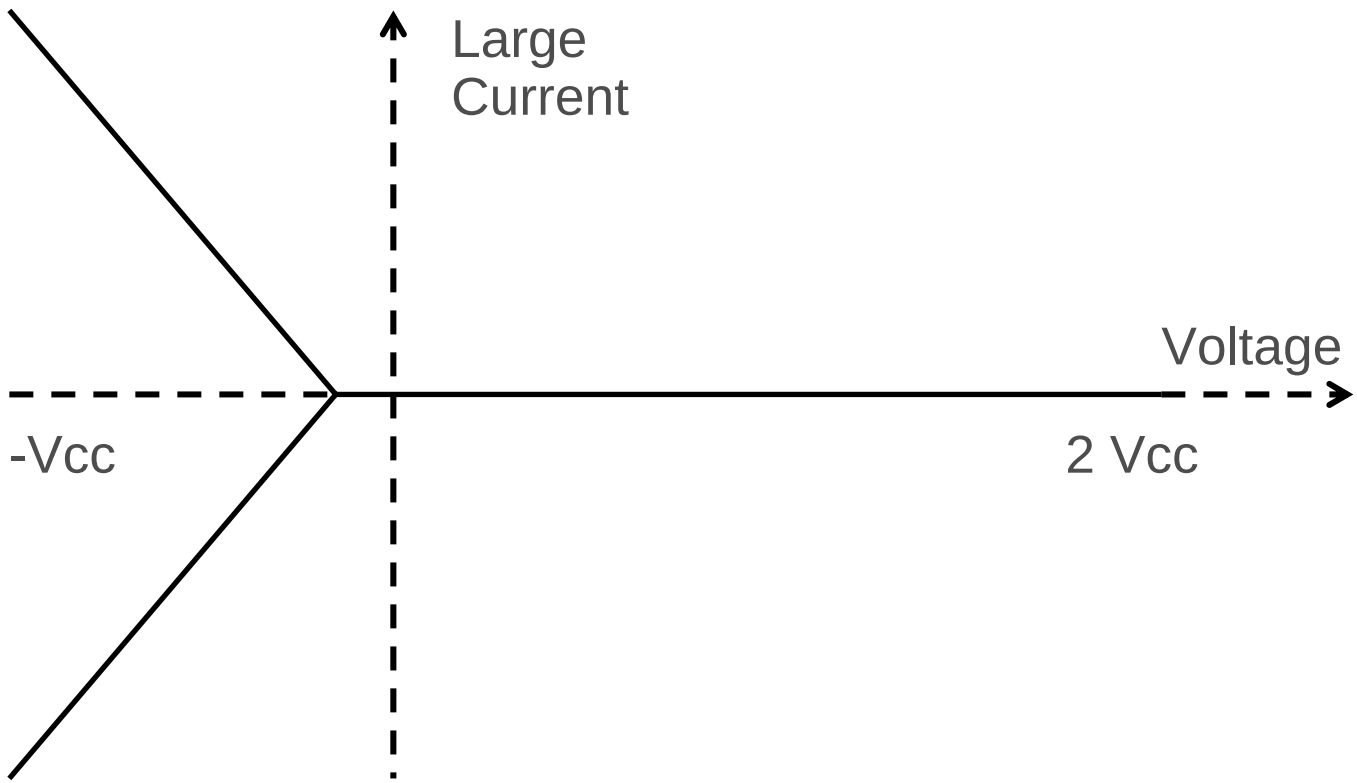
- V-t tables
  - Stop time => steady-state voltage reached
  - Time step < 0.10 * T_{edge}
  - DC voltages (Typ/Min/Max)
  - Data step (Core edge rate) (Typ/Min/Max)
  - Specified load (such as 50 Ohms)

Generating Table Data

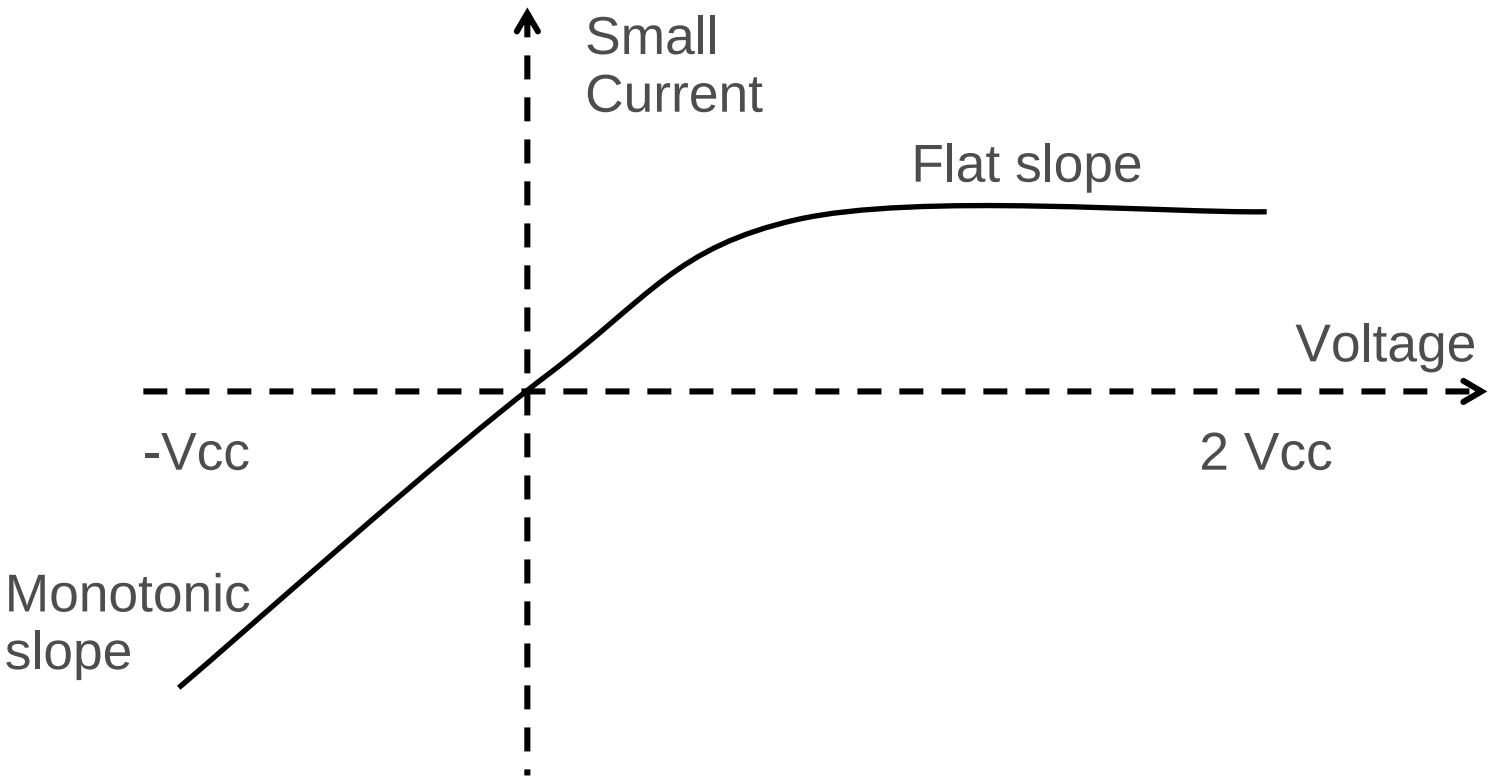
- Set of four V-t tables
  - Data rising, V_fixture=0
  - Data rising, V_fixture=Vcc
  - Data falling, V_fixture=0
  - Data falling, V_fixture=Vcc
- Output crosses through Vmeas



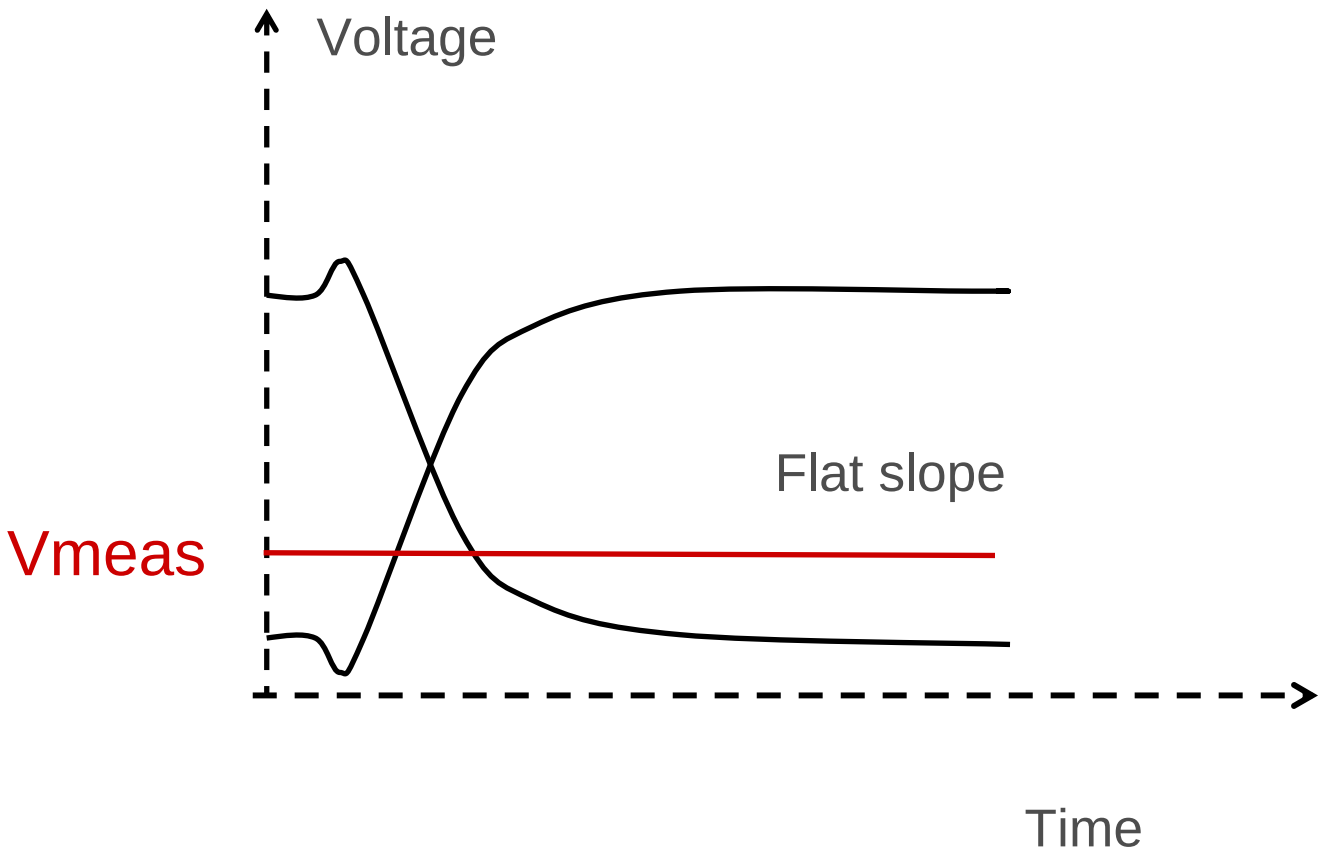
IBIS Tables: Graphical View [Power Clamp] and [GND Clamp]



IBIS Tables: Graphical View [Pullup] and [Pulldown]

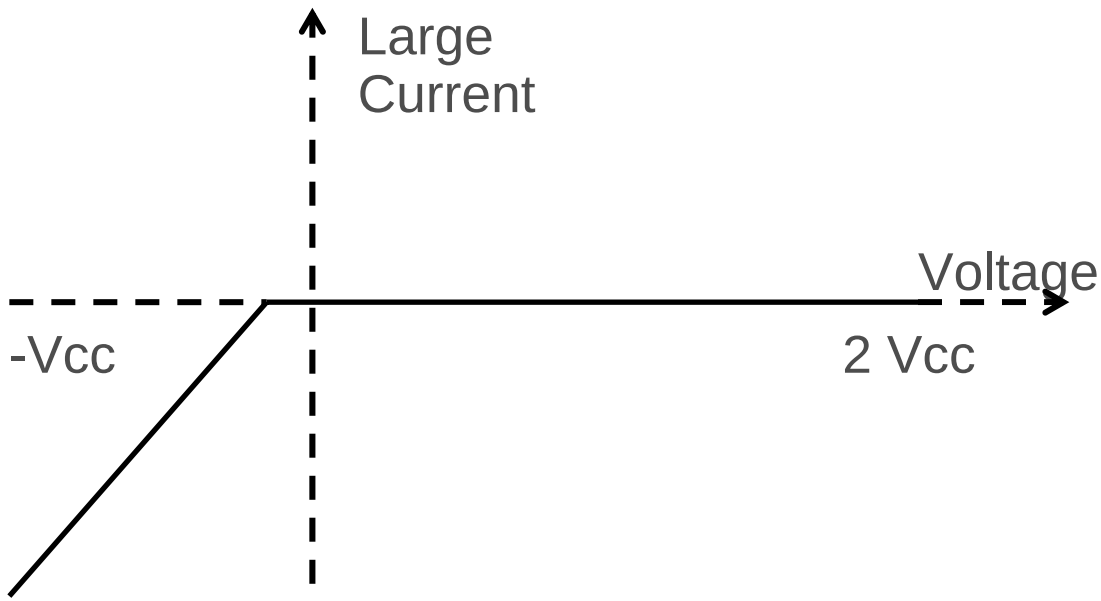


IBIS Tables: Graphical View
[Rising Waveform] and [Falling Waveform]



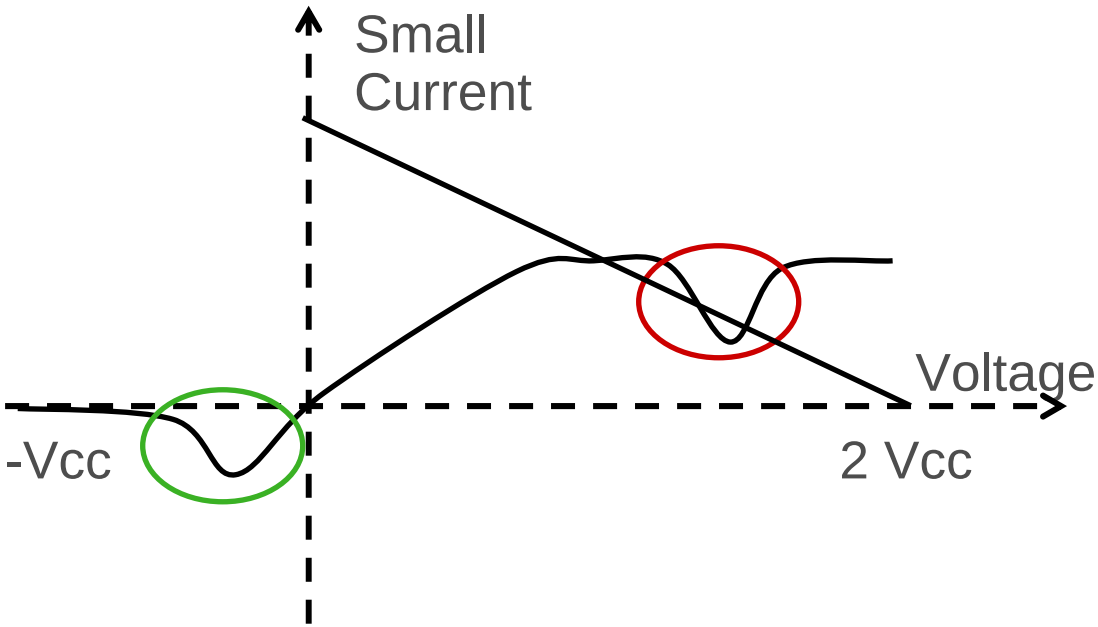
Common Problems
Power and GND clamp tables

- Little or no power clamp current
- Excessive current (kA to GA, even 1e18 Amps!)
- Table does not cover –Vcc to +Vcc



Common Problems
Pullup and Pulldown tables

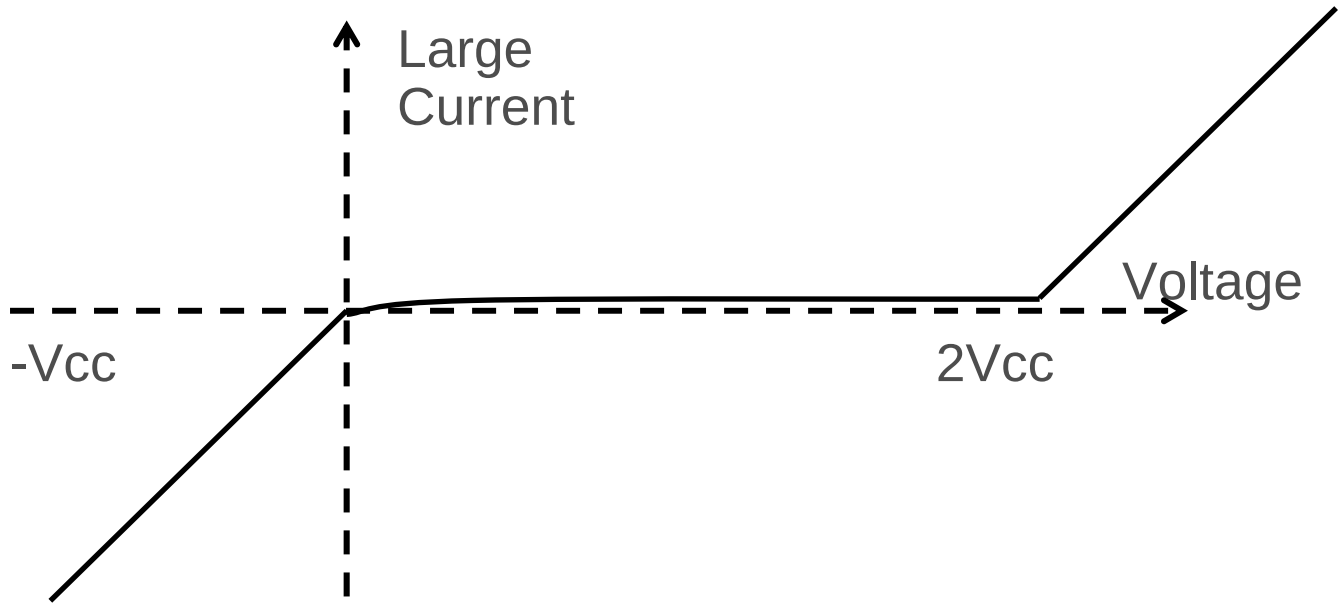
- Non-monotonic tables
- Table does not cover –Vcc to +2Vcc



Common Problems
Pullup and Pulldown tables

- Double counting of clamp currents
- Incorrect subtraction of clamp currents

```
I_dn = [GND clamp] + [Power clamp] + [Pulldown]
```



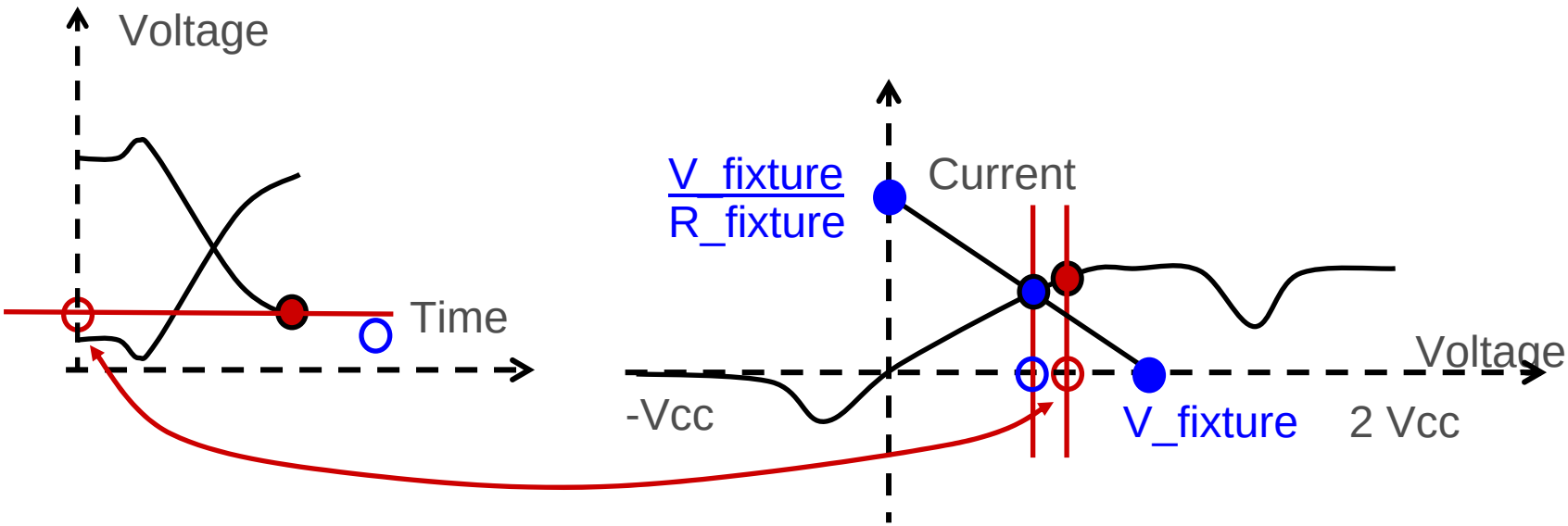
Common Problems
Rising and Falling V-t tables

- AC endpoint (DC point does not match I-V load line)

$$I\_fixture = \frac{V - V\_fixture}{R\_fixture}$$

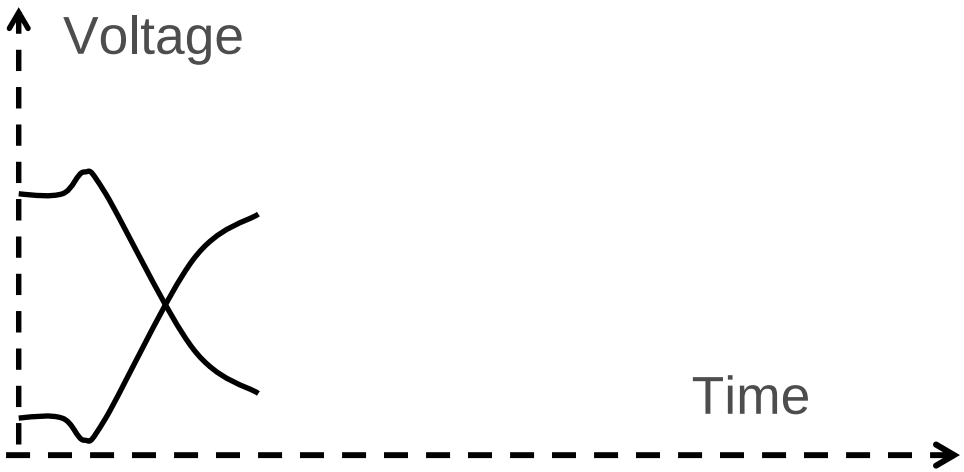
V at loadline with R_fixture

V @ I_fixture

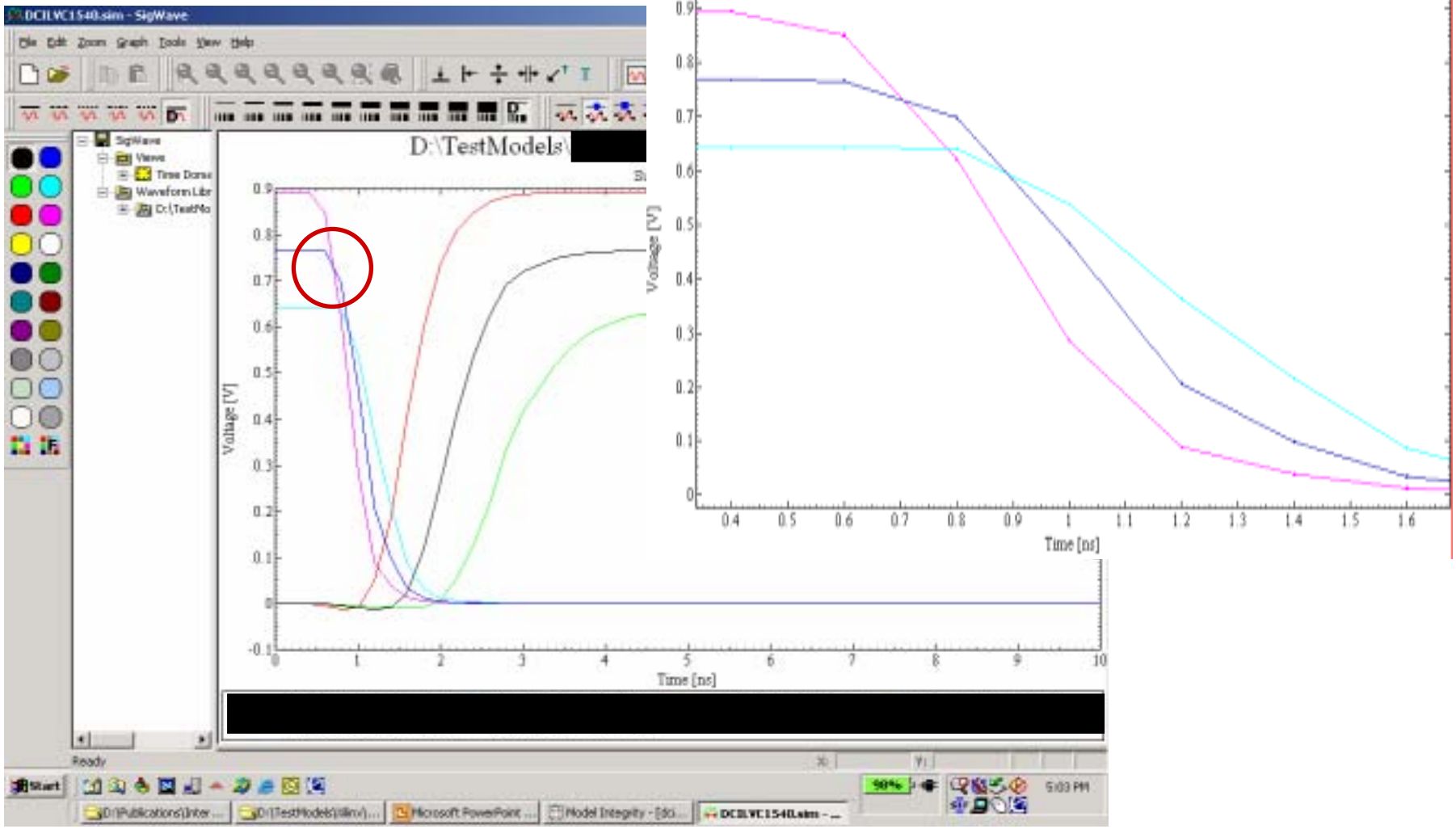


Common Problems
Rising and Falling V-t tables

- End slope not flat
- Tables not starting at same time
- Excessively long V-t tables
- Not enough points in the transition region
- Output does not cross Vmeas



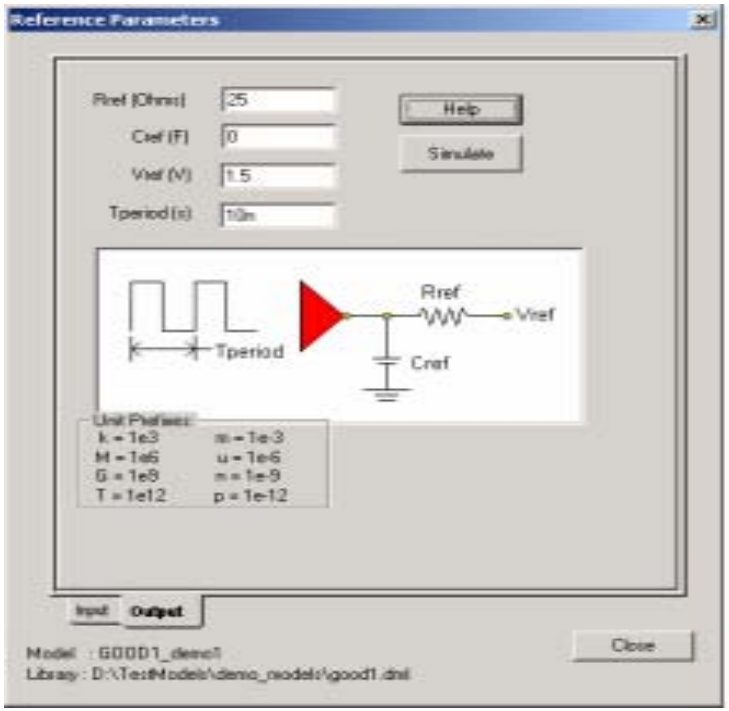
Common Problems
Best points selection

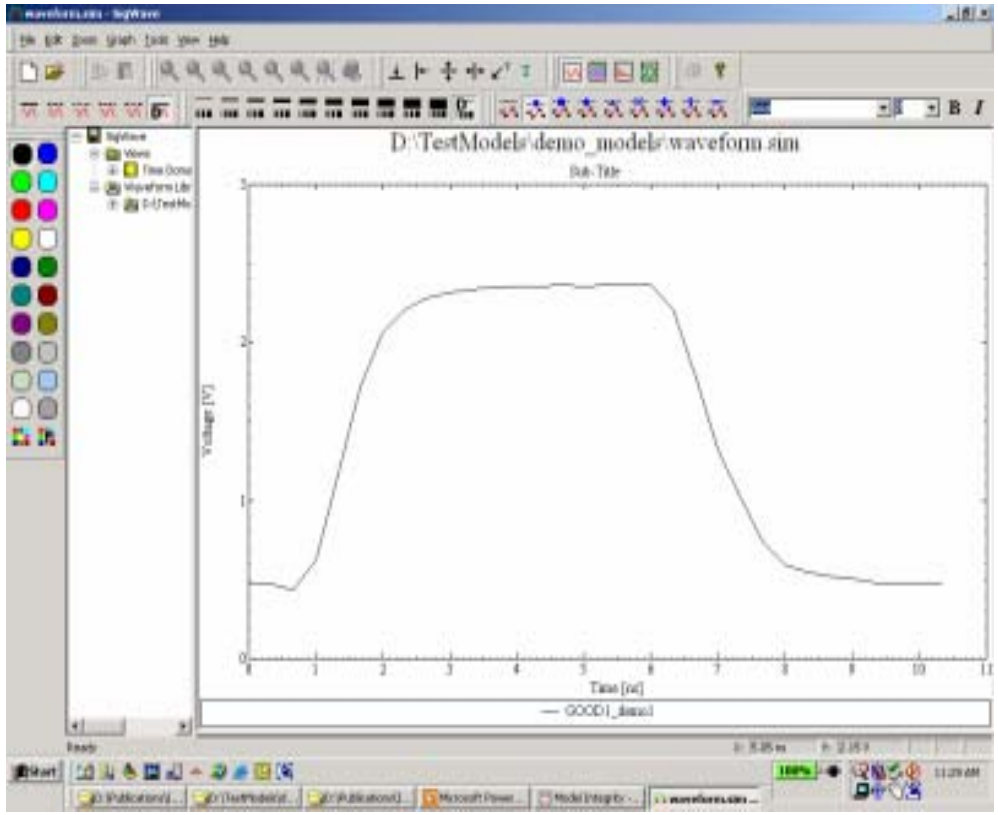


Addressing Common Problems
A Validation Methodology

- Parse to check syntax (ibischk3)
- Examine parameters
- View tables graphically
- Other data checks
- Simulate
- Release for design use
- Close the loop

Simulation





Addressing Common Problems
A Validation Methodology

- Identifying problems quickly takes experience
- Identifying problems easier with good tools
- Fixing problems requires judgment calls
  - When in doubt, users call the model maker!

Identifying Problems using Model Integrity (Demo)

Addressing Common Problems
A Validation Methodology

- Recent IBIS model validation presentations

http://www.cadencepcb.com/webinar/Modeling/frmModeling.asp

http://www.cadencepcb.com/webinar/Modeling2/frmModeling.asp

- Other links with IBIS validation and model creation papers

http://www.cadencepcb.com

http://www.eigroup.org/ibis/articles.htm

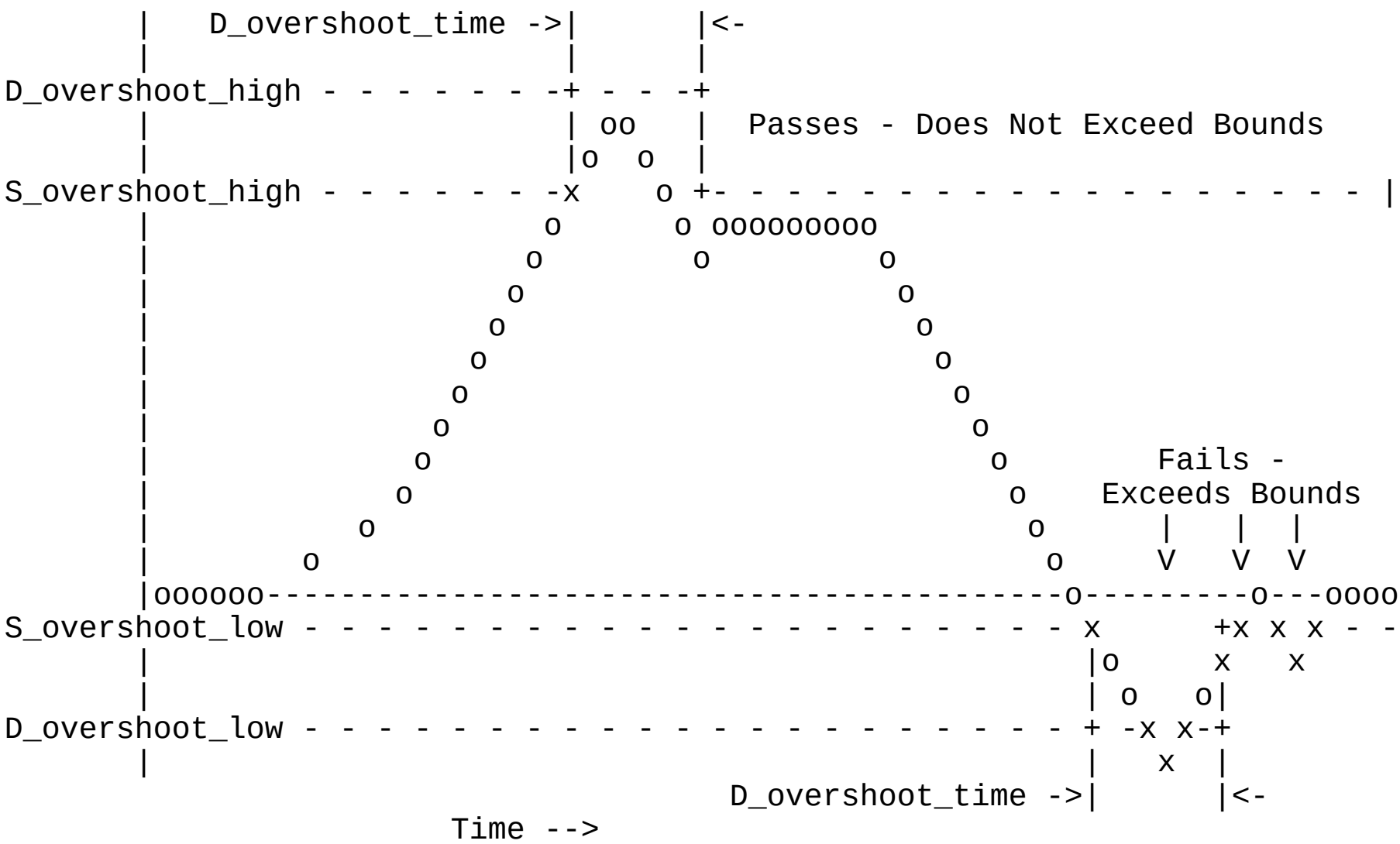
IBIS File Structure
I/O Buffer Models

- Advanced features
  - [Model Spec] : Timing parameters
  - [Submodel] : Dynamic_clamp, Bus_hold
  - [Driver Schedule] : Multi-stage driver
  - [TTgnd], [TTpower] : Clamp diode effects
- IBIS 4.0 adds
  - [Receiver Thresholds] : Input threshold parameters
  - External Reference] : DC voltage (for pseudo-differential)
  - [Add Submodel] : Adds Fall_back

IBIS File Structure
I/O Buffer Models

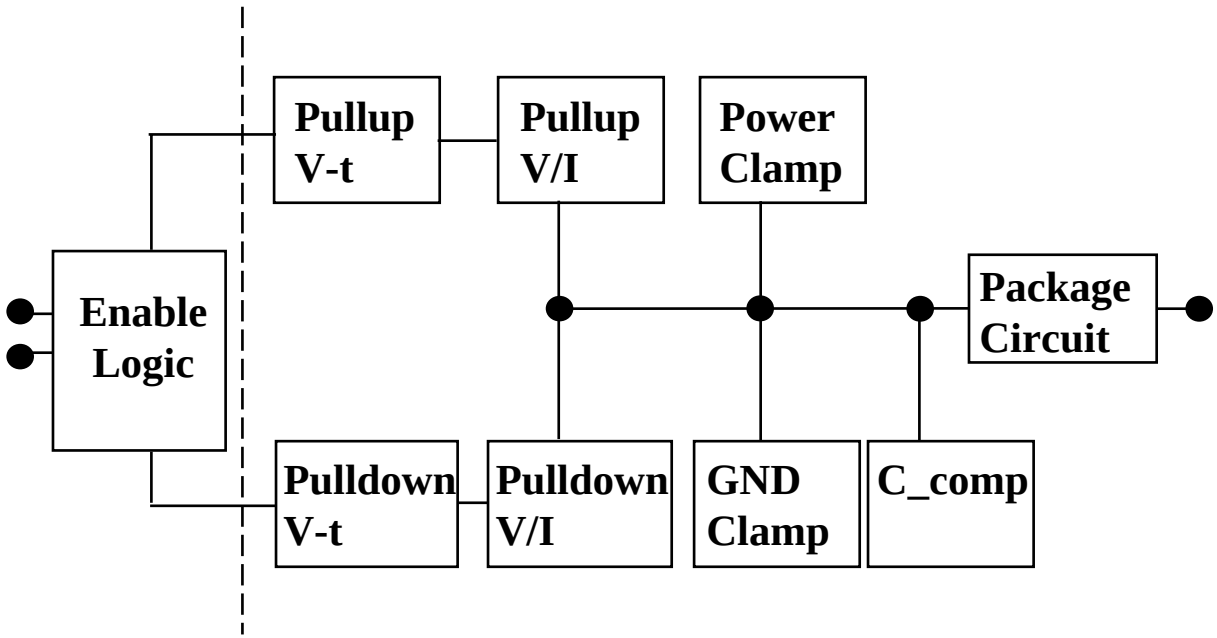
- [Model Spec] : Timing sub-params
  - Vinh, Vinl
  - Vinh+, Vinh-, Vinl+, Vinl-
  - S_overshoot_high, S_overshoot_low
    D_overshoot_high, D_overshoot_low, D_overshoot_time
    Pulse_high, Pulse_low, Pulse_time
  - Vmeas, Vref, Cref, Rref
  - Cref_rising, Cref_falling, Rref_rising, Rref_falling
    Vref_rising, Vref_falling, Vmeas_rising, Vmeas_falling
- These override [Model] sub-params
  - Vinh, Vinl, Vmeas, Vref, Cref, Rref

Static and Dynamic Checks



IBIS Data Interpretation

- I_down [GND clamp] + [Power clamp] + [Pulldown]
- I_up [GND clamp] + [Power clamp] + [Pullup]
- I_recvr [GND clamp] + [Power clamp]



IBIS File Structure
Series and Series Switch Models

- Calling a Series model for the component
- Pins must be in [Pin] list

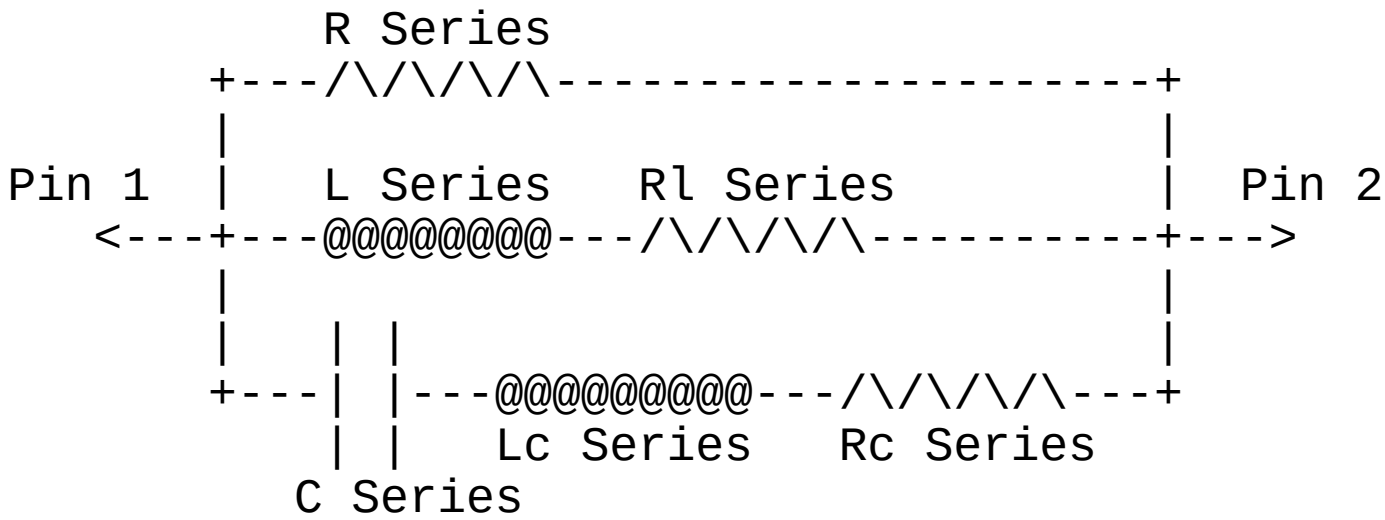
```
[Series Pin Mapping]  pin_2  model_name  function_table_group
|
 2     3      CBTSeries       1   | Four independent groups
 5     6      CBTSeries       2
 9     8      CBTSeries       3
 12   11      CBTSeries       4
|
 32   33      Fixed_series        | No group needed
|
[Series Switch Groups]           | Function Group States
On 1 2 3 /     | Default = ON
Off 4 /        | Default = OFF
```

IBIS File Structure
Series model types

- Series and Series_switch models
- Series model always On
- Series-switch state set at simulation time
  - [On], [Off]
  - Used with each Series_switch model type

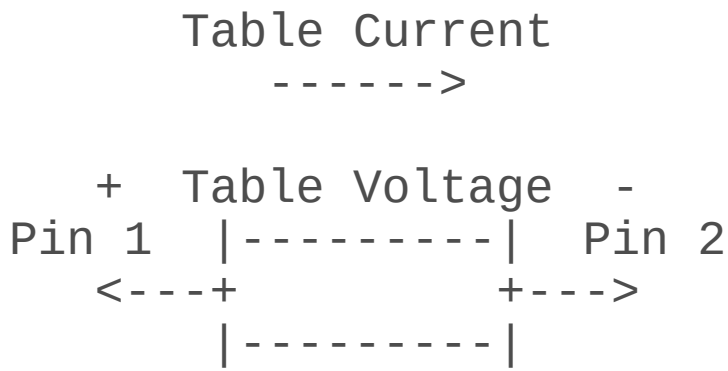
IBIS File Structure
Series model types

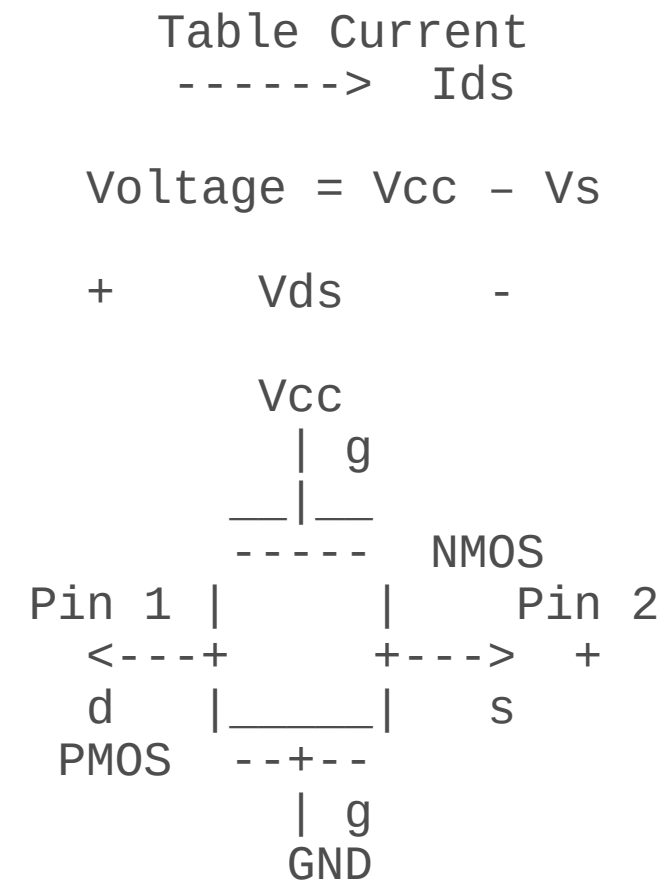
- Fixed value series components
  - [R Series]
  - [L Series], [Rl Series]
  - [C Series], [Lc Series], [Rc Series]
- Pins on the same component



IBIS File Structure
Series model types

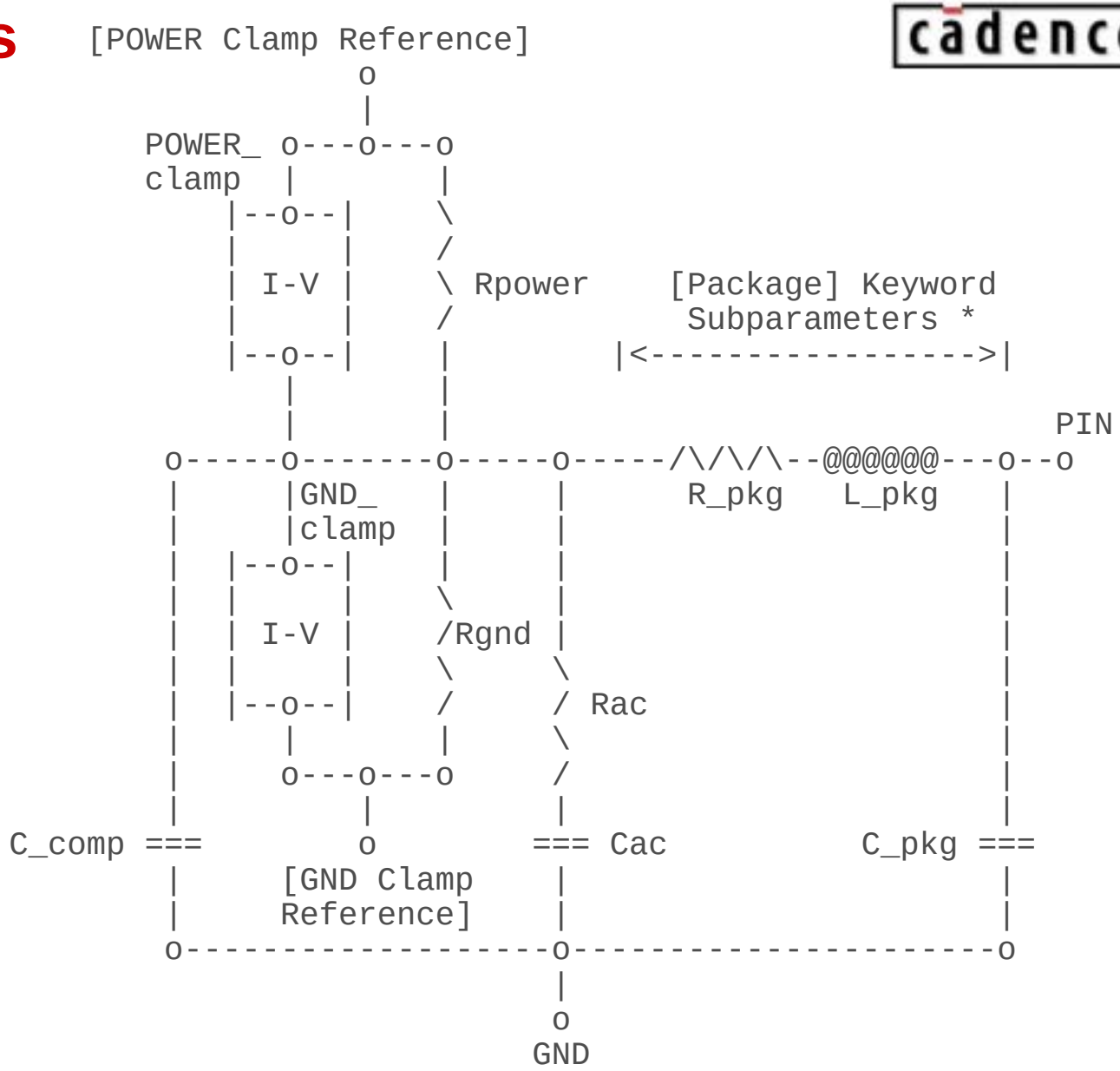
- [Series Current]
  - One I-V table
- [Series MOSFET]
  - Multiple I-V tables
  - One table for each Vgs





Terminators

- [Rgnd]
- [Rpower]
- [Rac]
- [Cac]



Module and Board Models

- EBD model
  - Simple transmission lines (L/R/C per unit length)
  - Lumped R, L, C elements
  - IC pin attachment
- PKG model
  - Adds RLC matrices for coupled lines
- Interconnect model (draft)
  - Adds S-parameter support

Summary

- IBIS Model Files
- Components and Models
- Identifying Common Problems
- Model Creation
- A Validation Methodology

IBIS Links

- Home Page http://www.eigroup.org/ibis/ibis.htm
- Specifications http://www.eigroup.org/ibis/specs.htm

  Also Cookbook and BIRDs
- Parser http://www.eda.org/pub/ibis/ibischk3/
- IBIS Summit papers http://www.eigroup.org/ibis/articles.htm

  Also Training Materials
- Quality Checklist (draft) http://www.sisoft.com/ibis-quality/checklist/
- FREE Model Reviews http://www.eigroup.org/ibis/support.htm

Cadence Links

- Cadence Home Page http://www.cadence.com
- SPECCTRAQuest Community http://www.specctraquest.com/
  - Papers, Webinars, Movies, Discussion threads
  - At least 75 hits on “IBIS”
  - Examples:
    - IBIS & SI at 3COM
    - IBIS Made Easy
    - Getting & Using IBIS Models - Tips & Tricks at CommWorks
    - Differential Buffer in the Form of Simulator-specific IBIS
    - IBIS: Table-based I/O Models
    - V-T Tables in IBIS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