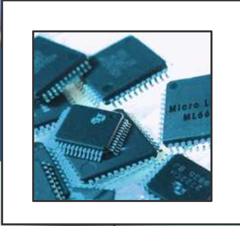


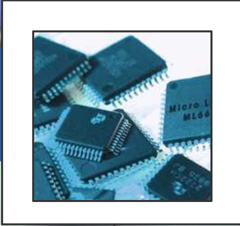
# A Method of Identifying Analog Cell Mismatch Issues Caused by Photo Mask Misalignment


David Schwan

Manager: CAD and Layout

Micro Linear


Micro Linear



# The Problem

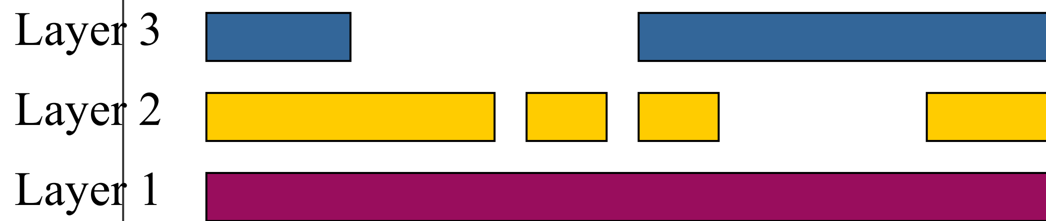
a) The IC fabrication process uses Photomasks.

b) Masks are aligned either to a “Zero Layer” or to the previous layer.

c) Alignment is subject to variation in X and Y directions, and will be obey normal statistical distributions

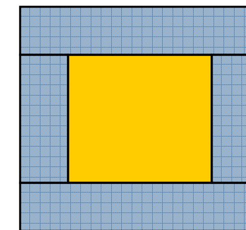
d) These variations can cause mismatches in analog circuits.

# Mask Layers and Alignment

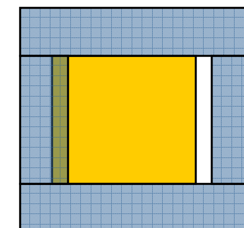


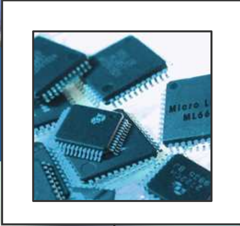

Vertical stacking of Layers

Perfect Alignment

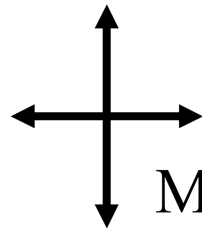


Allowed Misalignment

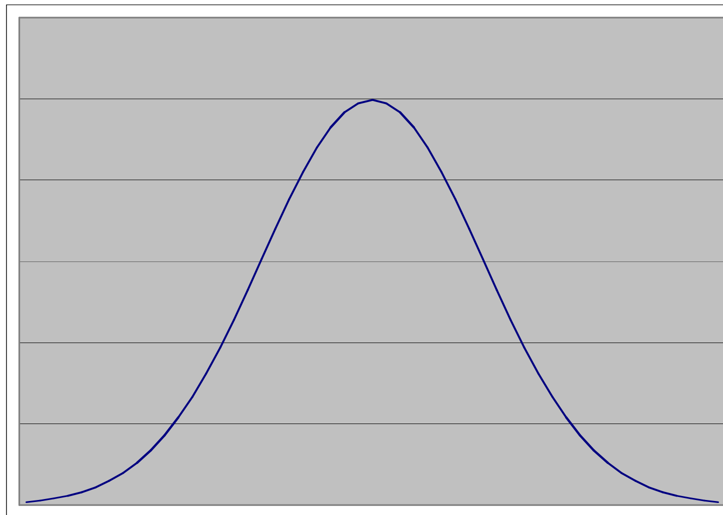


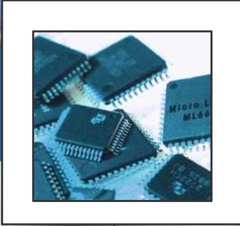


# Allowed Misalignment follows Normal  Distribution



Misalignment can be both X and Y, and follows a Normal Distribution





# Differential circuits are used for Noise Immunity

a) High performance analog systems use differential signals.

b) Differential signal paths offer high noise immunity because their balanced nature cancels out noise.

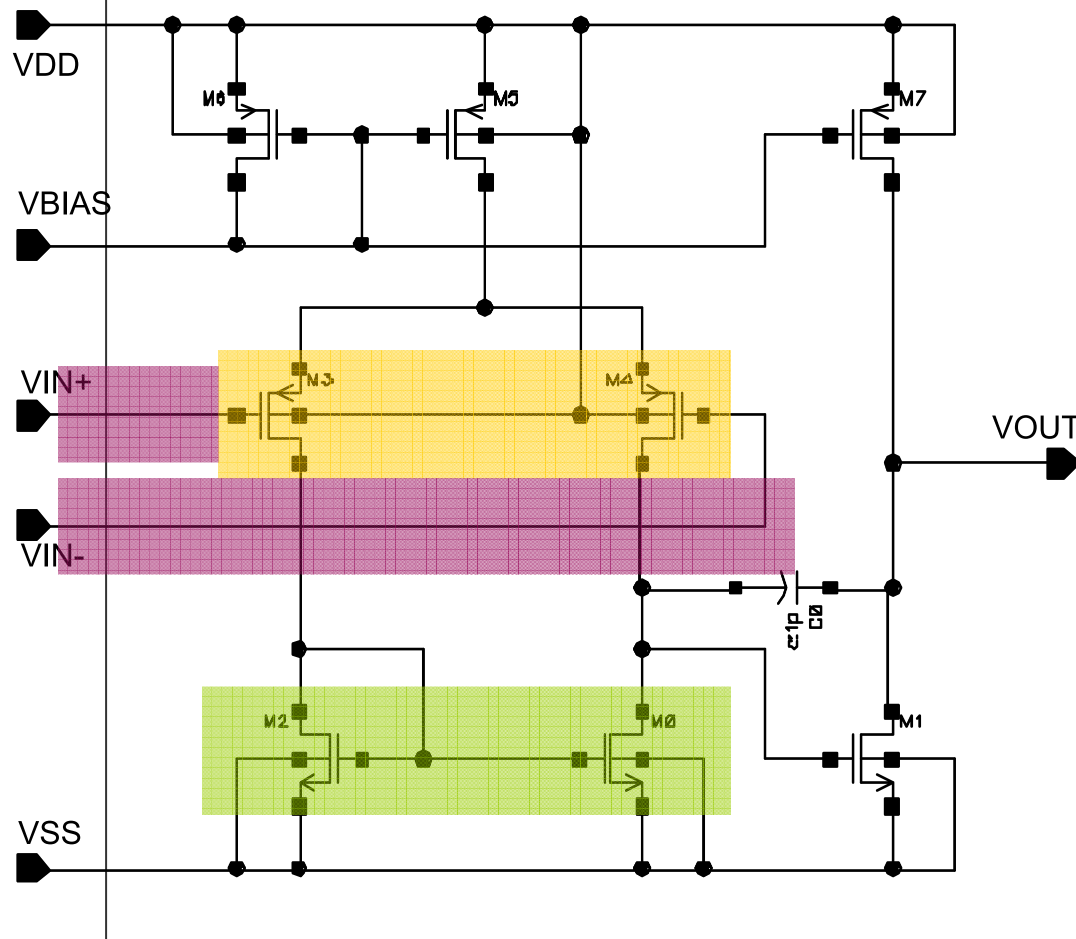
c) Differential signal paths can be poorly designed, and subsequently can show worse performance than a non-differential signal path.

d) Mismatching lowers overall system performance.

e) Transistors can be mismatched.

f) Interconnect can be mismatched.

# A Simple Op Amp - Differential input

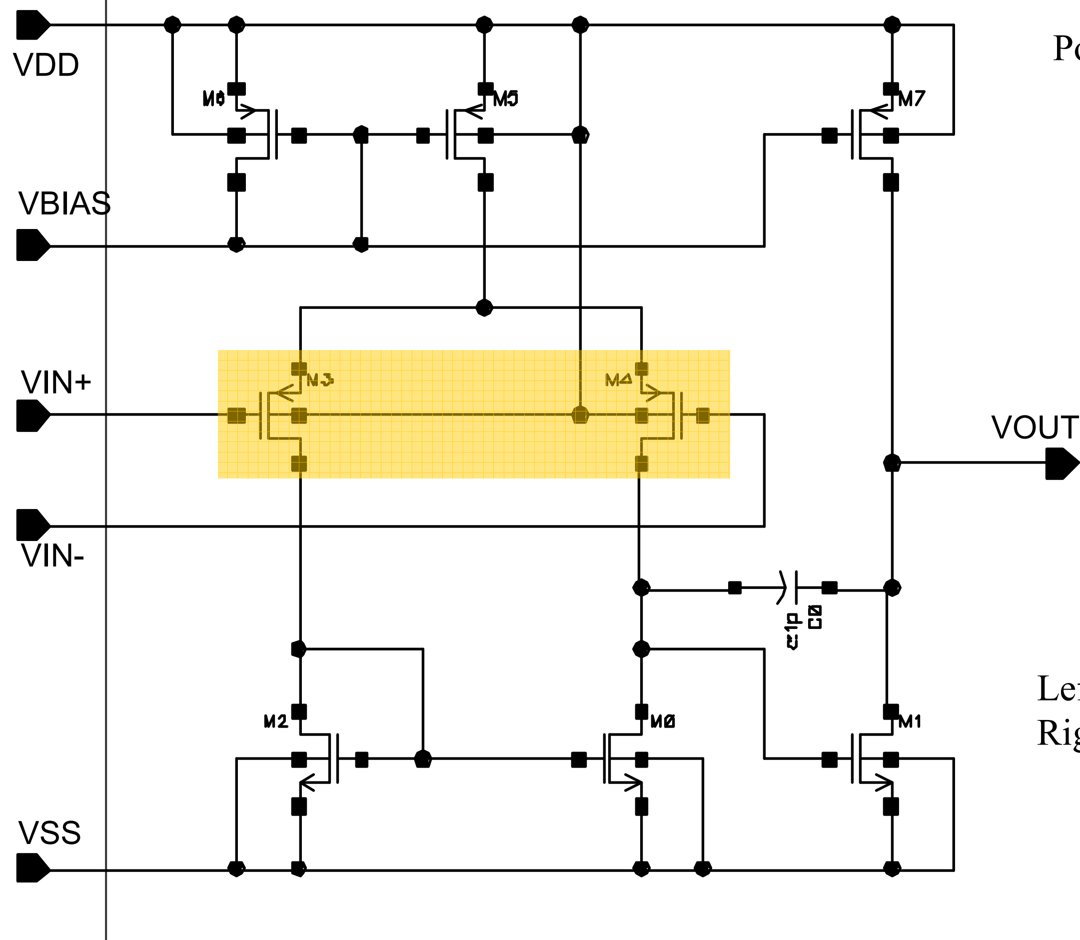


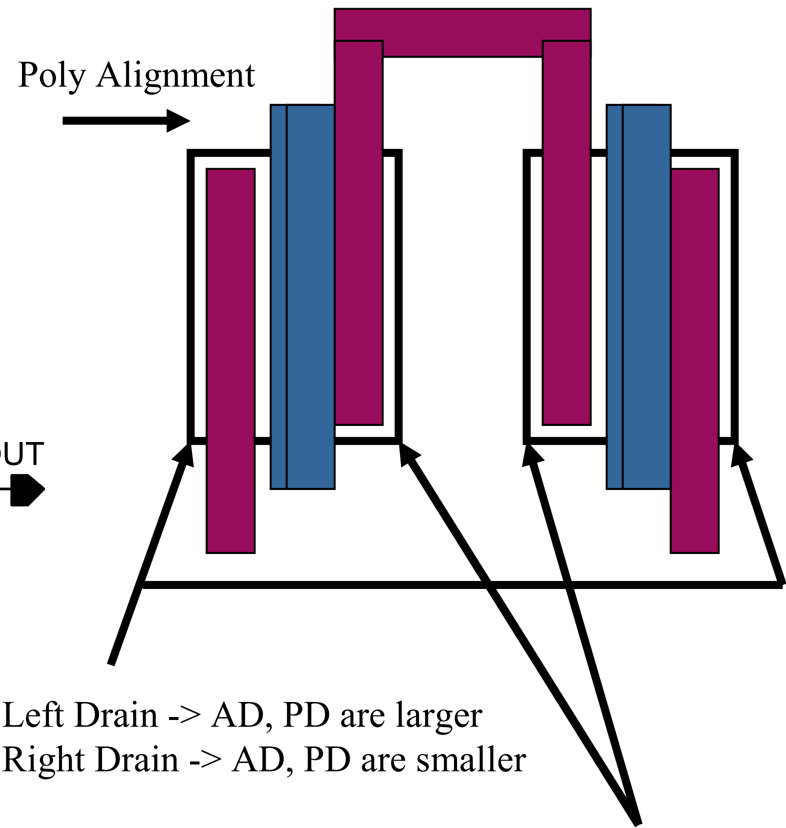

Input differential pair needs good matching.

Bias transistors need good matching.

Interconnect to differential pair transistors needs to be well matched.

# Mirrored Devices are not Matched

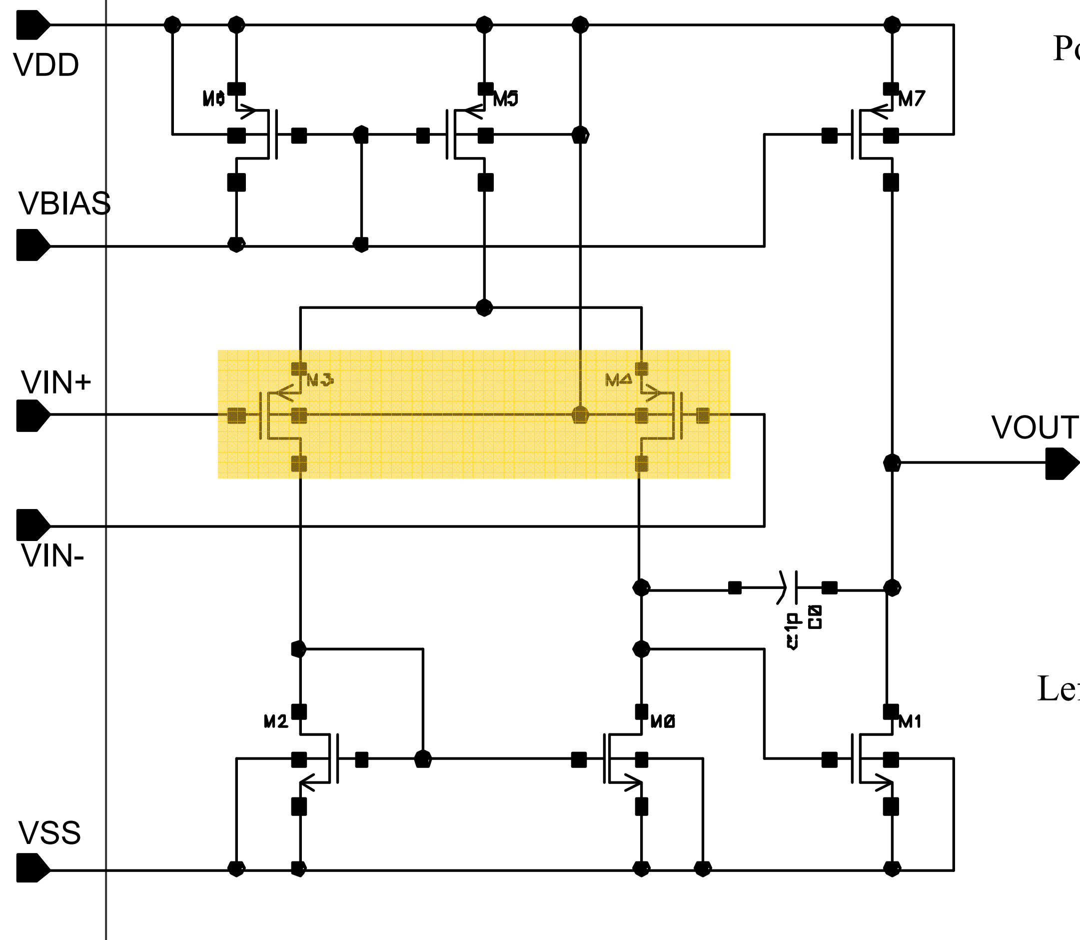


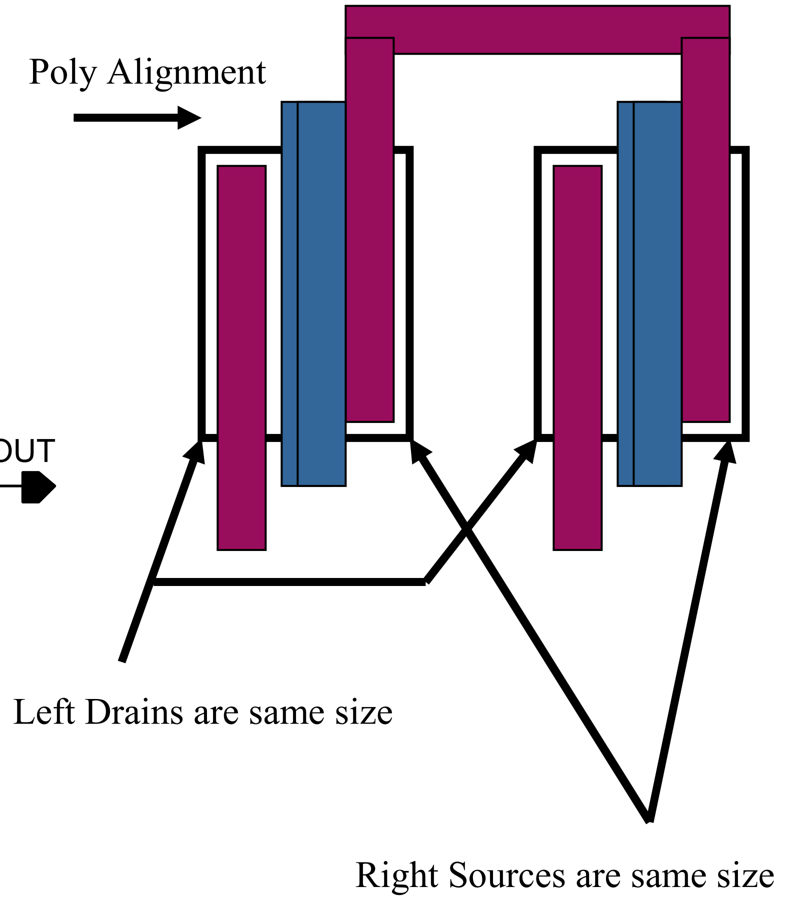




Left Drain -> AD, PD are larger
Right Drain -> AD, PD are smaller

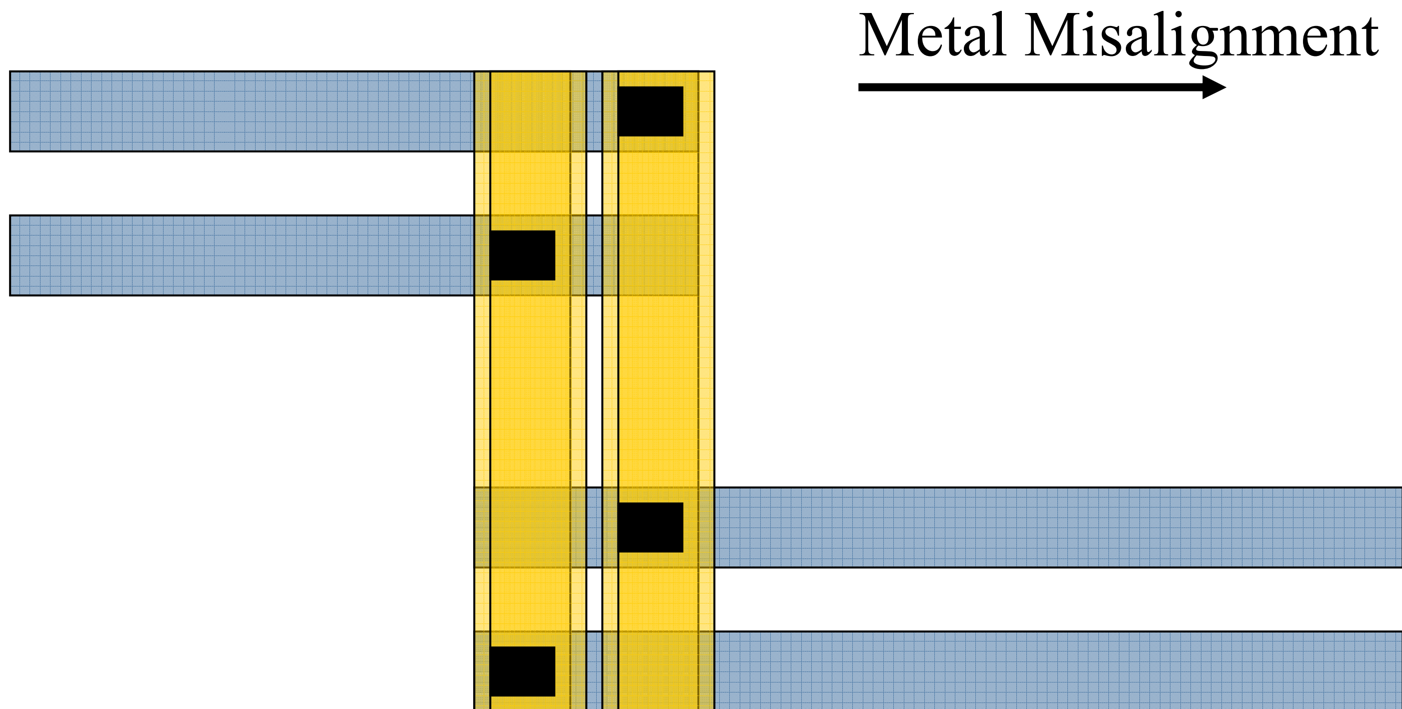
Left Source -> AS, PS are smaller
Right Source -> AS, PS are larger

# Stepped devices are Matched

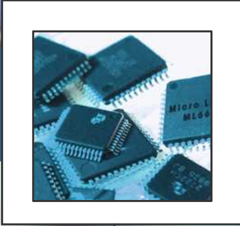


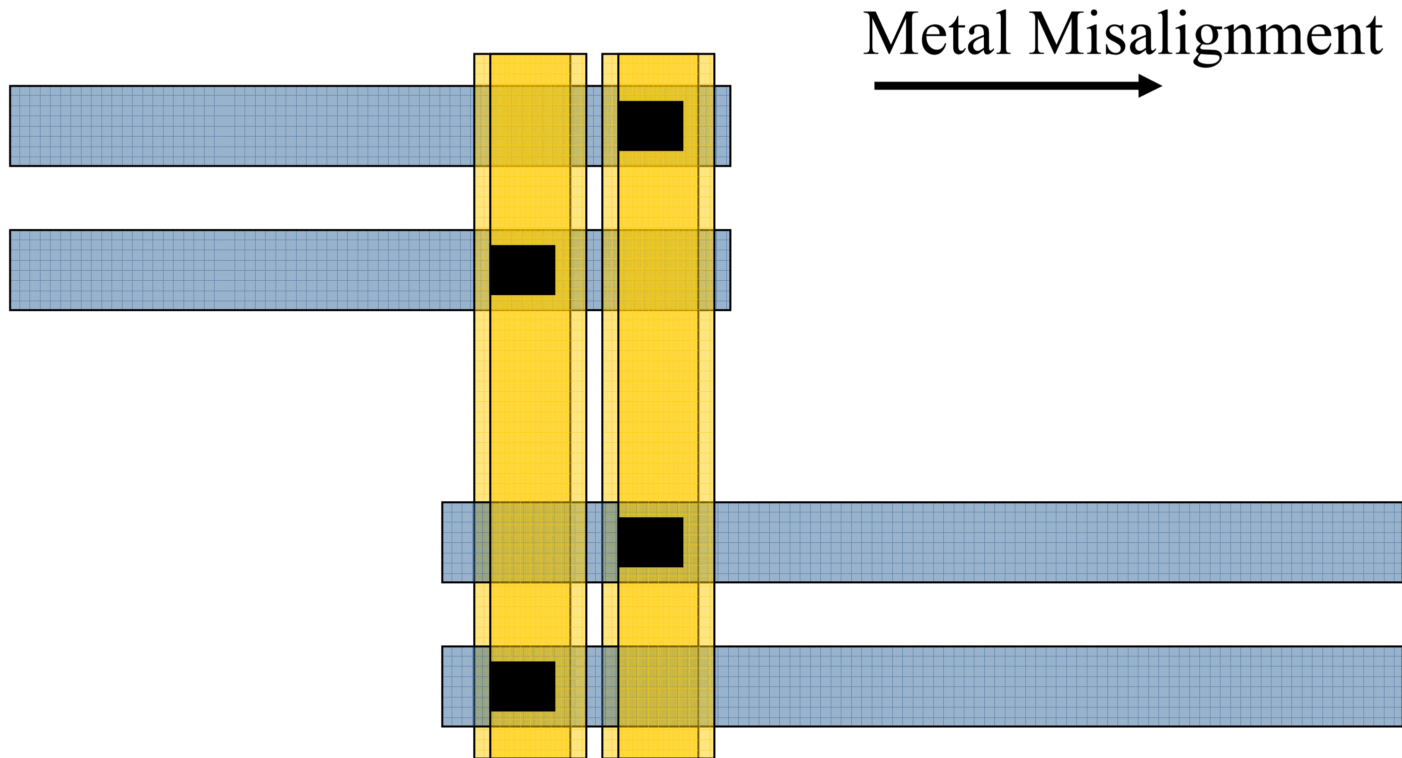
# Interconnect is subject to matching problems



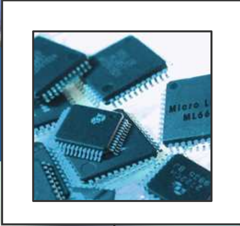

Differential interconnect with misalignment sensitivity



# Interconnect is subject to matching problems




Adding endcaps on upper and lower metal layers eliminates misalignment sensitivity.



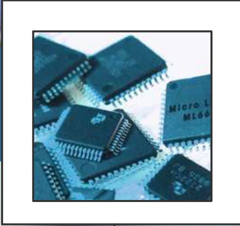
# Impact of mask misalignment

a) Mismatch due to misalignment is not found by running Monte Carlo simulations.

b) Conventional RC extraction assumes perfect mask alignment.

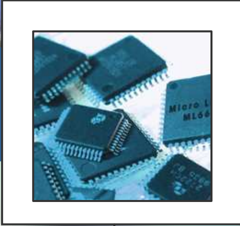
c) Misalignment creates systemic mismatches.

d) Circuit will function, but yield will follow normal distribution.



# The Solution

a) Circuit should start with RC extracted layout being properly balanced.
b) Only differences in capacitance and MOS AD, AS, PD, and PS are looked at.
c) Assura C extraction is used.
d) The geomShift command is used to simulate the mask misalignment.
e) Spice netlist is generated because it is easier to parse in a perl script.
f) Extraction is flat (no hierarchy) to simplify netlist postprocessing.



# The geomShift command

Outlayer = geomShift( inlayer, X shift, Y Shift)

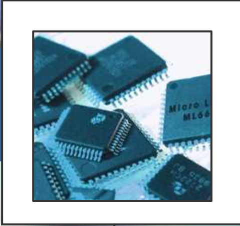
Rule Deck is modified so that input layer(s) are renamed, including the pin layers. Example:

met1 = layer("met1" type("drawing")) -> met1_mask_misalign = layer("met1" type("drawing"))

After the layerDefs, insert the geomShift command(s).

Met1 = geomShift(met1_mask_misalign, 0, 0.05)

This methodology allows the rest of rule deck to be unmodified.

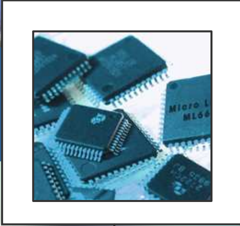


# Modify the extract.rul file

a) The extract.rul file is modified.

b) A perl script can be used to create the variant extract.rul files.

c) The techRuleSets file is modified to add each layer shift variant. Label each variant, by adding "- layer_name {up, down, left, right}" example: "RCX - Metal1 up"



# Run the “C” extractions

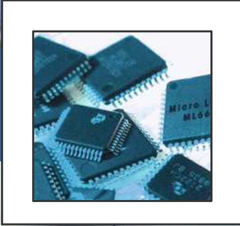
a) Run unshifted LVS, and “C” extraction.

b) Use .rsf files (lvs and rcx) as templates to run shifted jobs. Create new lvs.rsf file and rcx.rsf file. Within the appropriate .rsf file replace ?techRuleSet value with the appropriate layer shifted version. Example:

?techRuleSet “RCX” -> ?techRuleSet “RCX - Metal1 up”

Replace ?output with unique name, example:

?output “{runName.sp}” -> ?output “{runName}_Metal1_up.sp”

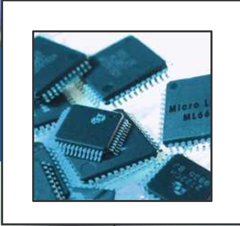


# Create script to run all shift jobs

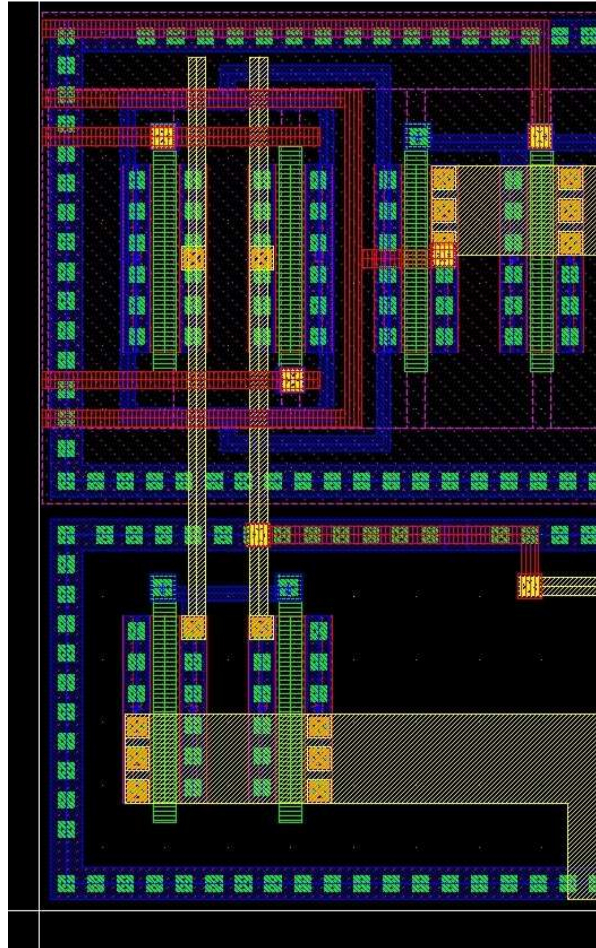
Example script:

<run_directory>/assura {runName}_Metal1_up.rsf
<run_directory>/assura rcx.{runName}Metal1_up.rsf
<run_directory>/assura {runName}_Metal1_down.rsf
<run_directory>/assura rcx.{runName}Metal1_down.rsf
<run_directory>/assura {runName}_Metal1_left.rsf
<run_directory>/assura rcx.{runName}Metal1_left.rsf
<run_directory>/assura {runName}_Metal1_right.rsf
<run_directory>/assura rcx.{runName}Metal1_right.rsf

This script should be run from the directory icfb is run from.



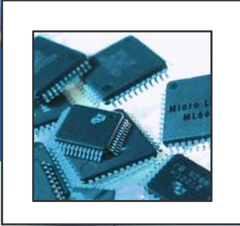
# Sample Case: Improper layout of differential pair



Input differential pair layout is sensitive to mask misalignment along with current sources for diff pair, both have mirrored (in x direction) layout.

Only poly misalignment is extracted.

For illustration purposes misalignment has been set at half the distance from Source/Drain contact to Gate.



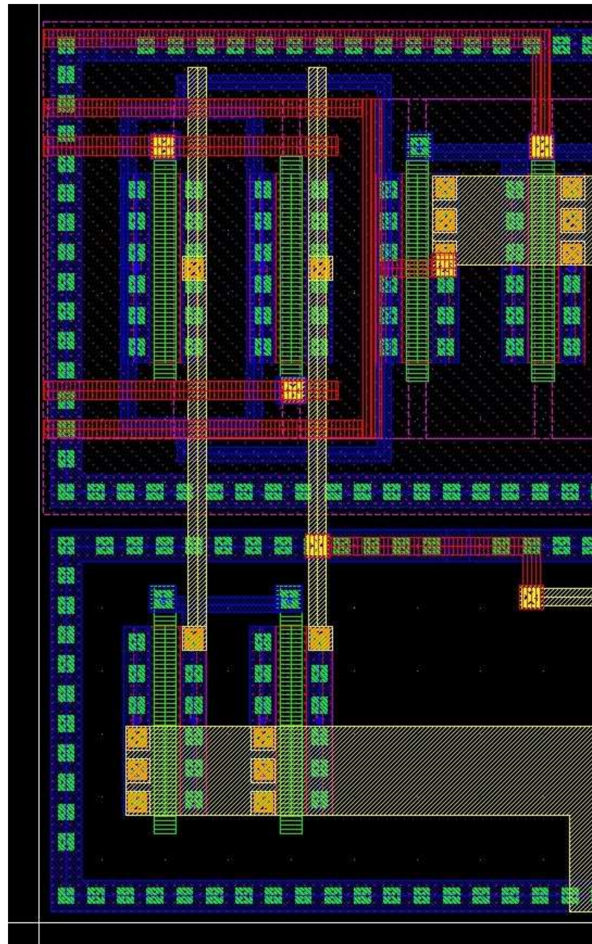
# Results: Sample Case: Improper layout of differential pair

| Case | Device | ad | as | pd | ps | nrd | nrs |
|---|---|---|---|---|---|---|---|
| **Original** | M4 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M3 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M2 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M0 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| **Poly Left** | M4 | ad=1.68P | as=1.2P | pd=7.12U | ps=6.8U | nrd=8.017E-02 | nrs=2.684E-02 |
| | M3 | ad=1.2P | as=1.68P | pd=6.8U | ps=7.12U | nrd=2.684E-02 | nrs=8.017E-02 |
| | M2 | ad=1.68P | as=1.2P | pd=7.12U | ps=6.8U | nrd=8.017E-02 | nrs=2.684E-02 |
| | M0 | ad=1.2P | as=1.68P | pd=6.8U | ps=7.12U | nrd=2.684E-02 | nrs=8.017E-02 |
| **Poly Right** | M4 | ad=1.2P | as=1.68P | pd=6.8U | ps=7.12U | nrd=2.684E-02 | nrs=8.017E-02 |
| | M3 | ad=1.68P | as=1.2P | pd=7.12U | ps=6.8U | nrd=8.017E-02 | nrs=2.684E-02 |
| | M2 | ad=1.2P | as=1.68P | pd=6.8U | ps=7.12U | nrd=2.684E-02 | nrs=8.017E-02 |
| | M0 | ad=1.68P | as=1.2P | pd=7.12U | ps=6.8U | nrd=8.017E-02 | nrs=2.684E-02 |
| **Poly Up** | M4 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M3 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M2 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M0 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| **Poly Down** | M4 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M3 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M2 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M0 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |

**Notes:**

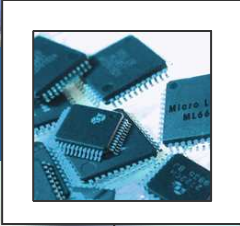
1) MOS device P-Cells have Source and Drain tagged.
2) Up and Down shift had no impact on MOS devices.
3) As expected matched pairs M4 <-> M3 and M2 <-> M0 have sources changing in opposite directions, and drains doing the same.

# Sample Case: Proper layout of differential pair



Input differential pair layout is insensitive to mask misalignment along with current sources for diff pair; both have stepped (in x direction) layout.

Only poly misalignment is extracted.

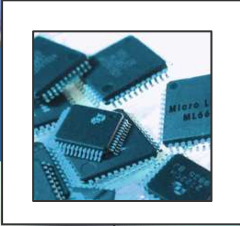


# Results: Sample Case: Proper layout of differential pair

| | Device | ad | as | pd | ps | nrd | nrs |
|---|---|---|---|---|---|---|---|
| **Original** | M4 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M3 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M2 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M0 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| **Poly Left** | M4 | ad=1.68P | as=1.2P | pd=7.12U | ps=6.8U | nrd=8.017E-02 | nrs=2.684E-02 |
| | M3 | ad=1.68P | as=1.2P | pd=7.12U | ps=6.8U | nrd=8.017E-02 | nrs=2.684E-02 |
| | M2 | ad=1.68P | as=1.2P | pd=7.12U | ps=6.8U | nrd=8.017E-02 | nrs=2.684E-02 |
| | M0 | ad=1.68P | as=1.2P | pd=7.12U | ps=6.8U | nrd=8.017E-02 | nrs=2.684E-02 |
| **Poly Right** | M4 | ad=1.2P | as=1.68P | pd=6.8U | ps=7.12U | nrd=2.684E-02 | nrs=8.017E-02 |
| | M3 | ad=1.2P | as=1.68P | pd=6.8U | ps=7.12U | nrd=2.684E-02 | nrs=8.017E-02 |
| | M2 | ad=1.2P | as=1.68P | pd=6.8U | ps=7.12U | nrd=2.684E-02 | nrs=8.017E-02 |
| | M0 | ad=1.2P | as=1.68P | pd=6.8U | ps=7.12U | nrd=2.684E-02 | nrs=8.017E-02 |
| **Poly Up** | M4 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M3 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M2 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M0 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| **Poly Down** | M4 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M3 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M2 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |
| | M0 | ad=1.44P | as=1.44P | pd=6.96U | ps=6.96U | nrd=5.354E-02 | nrs=5.354E-02 |

**Notes:**

1) MOS device P-Cells have Source and Drain tagged.
2) Up and Down shift had no impact on MOS devices.
3) As expected matched pairs M4 <-> M3 and M2 <-> M0 have sources changing in same direction, and drains doing the same.

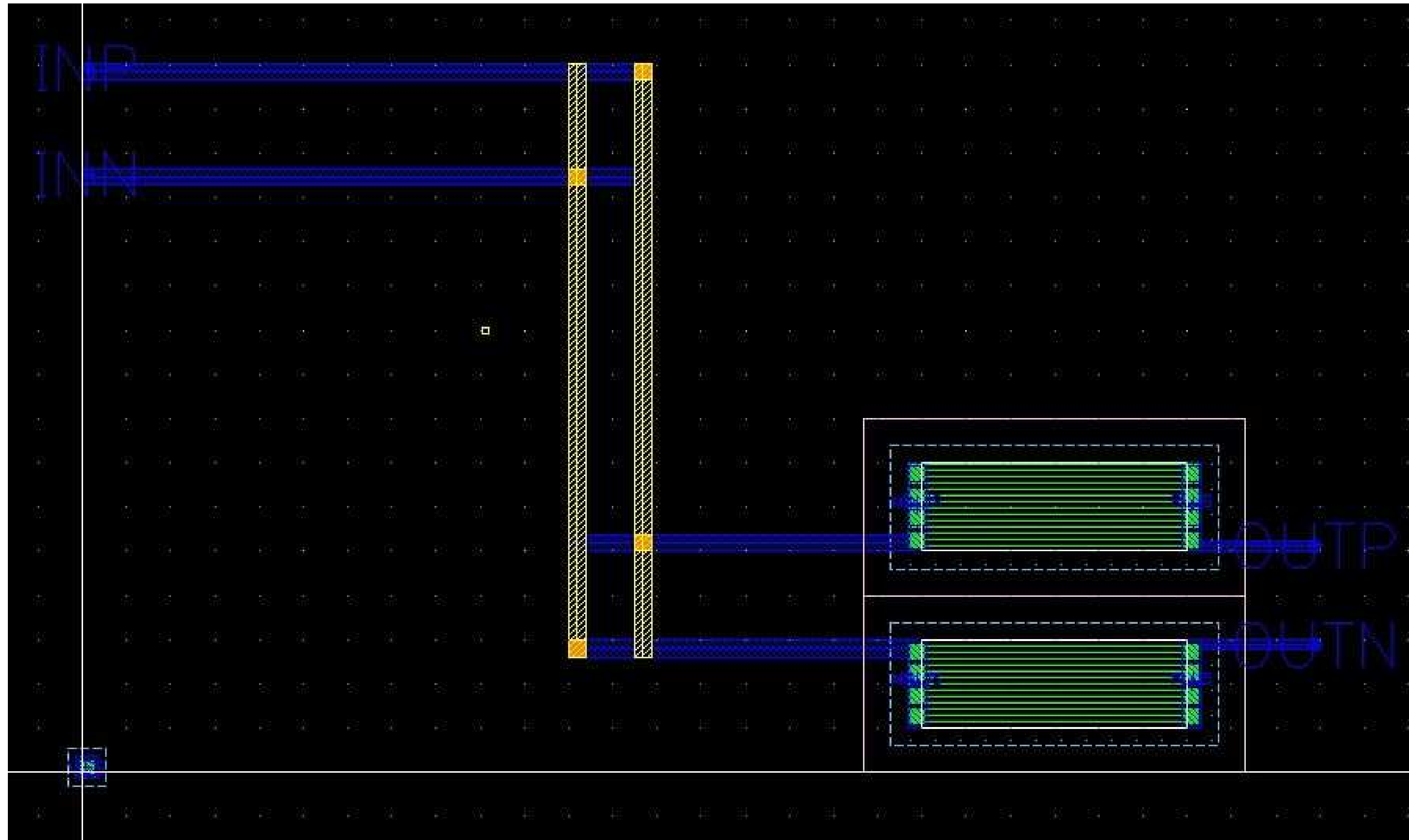


# Results: Sample Case: Proper layout of differential pair

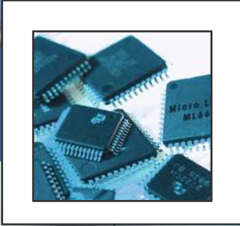
Note that stepped layout will have changed AD, AS, PD, and PS. The trick is making both sides of any differential pair move in the same direction. By moving the same way any offset moves in a similar manner and are cancelled out.

A design engineer may want to simulate the mask Misaligned extraction, to better tune the design to meet specifications.

# Sample Case: Bad Differential Interconnect



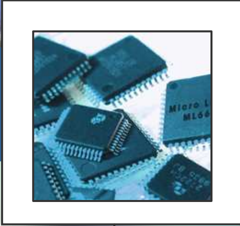

INP and INN need to see equivalent capacitance, layout above is subject to mask misalignment. Metal-1 and Metal-2 shifting done.



# Results: Sample Case: Bad Differential Interconnect

| | | | | |
|---|---|---|---|---|
| **Original** | c2 | OUTN | OUTP | 5.629E-17 |
| | c5 | OUTN | VSS | 5.218E-16 |
| | c6 | OUTP | VSS | 5.218E-16 |
| **Metal-1 Up** | c2 | OUTN | OUTP | 5.629E-17 |
| | c5 | OUTN | VSS | 5.218E-16 |
| | c6 | OUTP | VSS | 5.218E-16 |
| **Metal-1 Down** | c2 | OUTN | OUTP | 5.629E-17 |
| | c5 | OUTN | VSS | 5.218E-16 |
| | c6 | OUTP | VSS | 5.218E-16 |
| **Metal-1 Left** | c2 | OUTN | OUTP | 5.629E-17 |
| | c5 | OUTN | VSS | 5.218E-16 |
| | c6 | OUTP | VSS | 5.218E-16 |
| **Metal-1 Right** | c2 | OUTN | OUTP | 5.627E-17 |
| | c5 | OUTN | VSS | 5.217E-16 |
| | c6 | OUTP | VSS | 5.217E-16 |
| **Metal-2 Up** | c2 | OUTN | OUTP | 5.629E-17 |
| | c5 | OUTN | VSS | 5.218E-16 |
| | c6 | OUTP | VSS | 5.218E-16 |
| **Metal-2 Down** | c2 | OUTN | OUTP | 5.629E-17 |
| | c5 | OUTN | VSS | 5.218E-16 |
| | c6 | OUTP | VSS | 5.218E-16 |
| **Metal-2 Left** | c2 | OUTN | OUTP | 5.629E-17 |
| | c5 | OUTN | VSS | 5.218E-16 |
| | c6 | OUTP | VSS | 5.218E-16 |
| **Metal-2 Right** | c2 | OUTN | OUTP | 5.629E-17 |
| | c5 | OUTN | VSS | 5.218E-16 |
| | c6 | OUTP | VSS | 5.218E-16 |

OUTN and OUTP are not effected by mask misalignment, Which is consistent with starting layout.

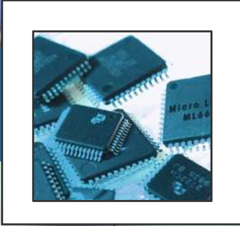


# Results: Sample Case: Bad Differential Interconnect

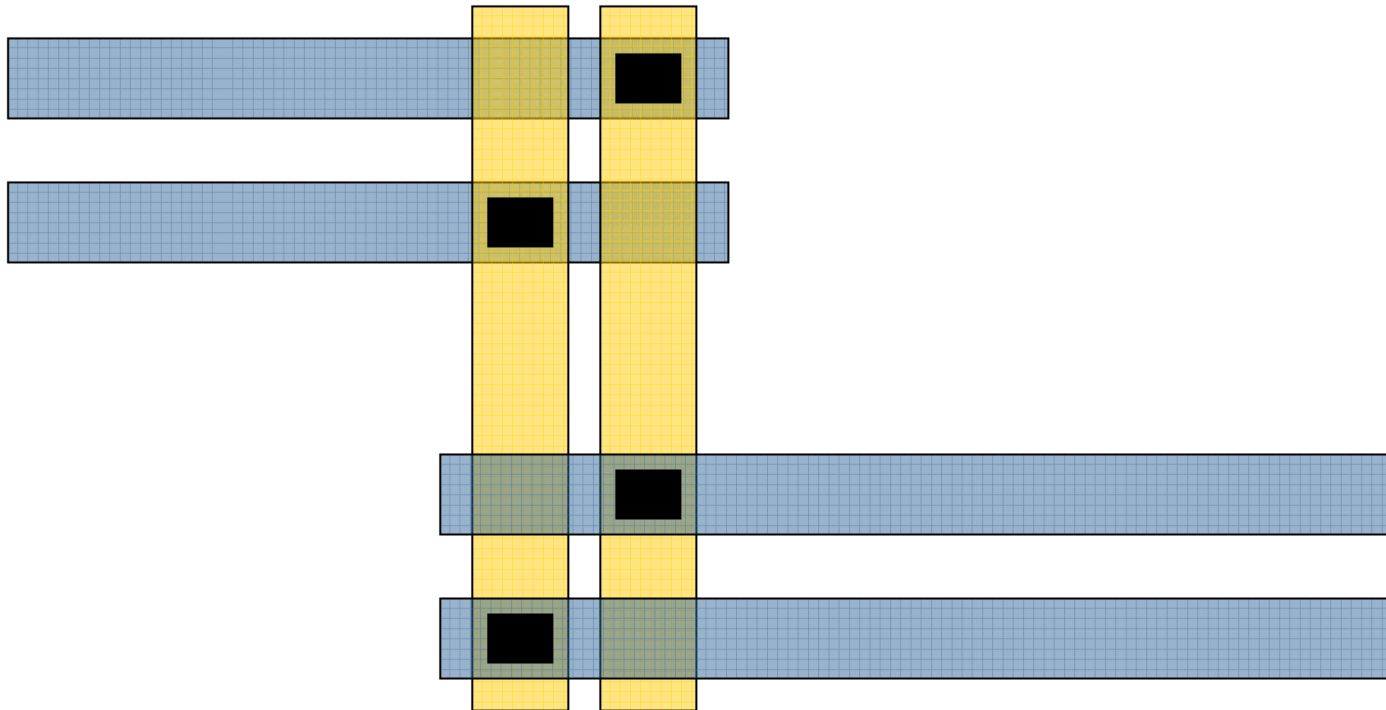
| | | | | |
|---|---|---|---|---|
| **Original** | c1 | INN | INP | 1.096E-15 |
| | c3 | INN | VSS | 2.725E-15 |
| | c4 | INP | VSS | 2.725E-15 |
| **Metal-1 Up** | c1 | INN | INP | 1.079E-15 |
| | c3 | INN | VSS | 2.738E-15 |
| | c4 | INP | VSS | 2.762E-15 |
| **Metal-1 Down** | c1 | INN | INP | 1.079E-15 |
| | c3 | INN | VSS | 2.762E-15 |
| | c4 | INP | VSS | 2.738E-15 |
| **Metal-1 Left** | c1 | INN | INP | 1.096E-15 |
| | c3 | INN | VSS | 2.740E-15 |
| | c4 | INP | VSS | 2.755E-15 |
| **Metal-1 Right** | c1 | INN | INP | 1.096E-15 |
| | c3 | INN | VSS | 2.755E-15 |
| | c4 | INP | VSS | 2.740E-15 |
| **Metal-2 Up** | c1 | INN | INP | 1.080E-15 |
| | c3 | INN | VSS | 2.763E-15 |
| | c4 | INP | VSS | 2.739E-15 |
| **Metal-2 Down** | c1 | INN | INP | 1.079E-15 |
| | c3 | INN | VSS | 2.738E-15 |
| | c4 | INP | VSS | 2.762E-15 |
| **Metal-2 Left** | c1 | INN | INP | 1.096E-15 |
| | c3 | INN | VSS | 2.755E-15 |
| | c4 | INP | VSS | 2.740E-15 |
| **Metal-2 Right** | c1 | INN | INP | 1.096E-15 |
| | c3 | INN | VSS | 2.740E-15 |
| | c4 | INP | VSS | 2.755E-15 |

We are concerned with differences between INN and INP, so we can ignore capacitor c1.

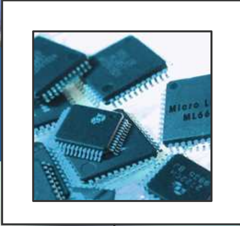
Capacitors c2 and c3 show that the inter-connect is subject to mask misalignment.



# Sample Case: Good Differential Interconnect



Endcaps are added on Metal-1 and Metal-2 traces INN and INP. The overhang is twice the Mask misalignment.

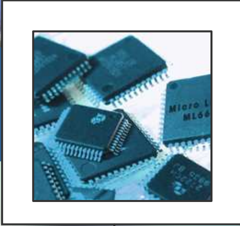


# Results: Sample Case: Good Differential Interconnect

| | | | | |
|---|---|---|---|---|
| **Original** | c3 | INN | VSS | 2.834E-15 |
| | c4 | INP | VSS | 2.834E-15 |
| **Metal-1 Up** | c3 | INN | VSS | 2.834E-15 |
| | c4 | INP | VSS | 2.835E-15 |
| **Metal-1 Down** | c3 | INN | VSS | 2.835E-15 |
| | c4 | INP | VSS | 2.834E-15 |
| **Metal-1 Left** | c3 | INN | VSS | 2.826E-15 |
| | c4 | INP | VSS | 2.828E-15 |
| **Metal-1 Right** | c3 | INN | VSS | 2.828E-15 |
| | c4 | INP | VSS | 2.826E-15 |
| **Metal-2 Up** | c3 | INN | VSS | 2.835E-15 |
| | c4 | INP | VSS | 2.835E-15 |
| **Metal-2 Down** | c3 | INN | VSS | 2.834E-15 |
| | c4 | INP | VSS | 2.835E-15 |
| **Metal-2 Left** | c3 | INN | VSS | 2.828E-15 |
| | c4 | INP | VSS | 2.826E-15 |
| **Metal-2 Right** | c3 | INN | VSS | 2.826E-15 |
| | c4 | INP | VSS | 2.828E-15 |

Still some mismatch, but smaller than without endcaps.

Mismatch can be further reduced by using longer endcaps.



# Conclusions

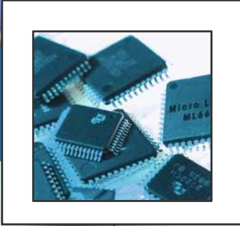
a) Mask Misalignment mismatches can be identified.

b) As feature size decreases, interconnect mask misalignment loses significance due to thickness of dielectric being greater than the same layer spacing.

c) Brute force method may limit applicablity to small circuits.

d) As number of metal layers increases, runtime goes up.

e) Currently no methods exist to automatically identify critical nodes in the design. Tools like Accelicon's AVP could be potentially used to identify the critical nets.



# Future Investigation

a) NPN’s are subject to misalignment mismatch, rule deck could be extended to include them.

b) Some of the variation in logic timing is due to misalignment. Creating layouts of standard cells with all transistors oriented in the same direction may have impact on the timing.

c) Parasitic Resistance is probably effected by mismatch, but the extraction may not be as easy.