Uncovering the Mystery of Sensor Circuits' Stability

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Abstract. Achieving stability is a way of life in analog circuit design. Though it could be a long way to learn the modern circuit stability theory and apply it to sensors, here is a shortcut.

After designing a sensor's circuit not long ago, I conducted an investigation on its stability. With an AC source at the circuit input I calculated the frequency response of the output. The sensor circuit seemed to show a sufficient phase margin. When tested in the lab, to my surprise, the sensor prototype would easily enter oscillation. To decipher the mystery of this amazing experience, thorough understanding the basics of circuit feedback theory is essential.

Over half a century ago Bode published the groundbreaking theory on circuit feedback and stability. Since then Bode's theory has steadily evolved to a modern science and a variety of state-of-the-art techniques for circuit design and evaluation. The circuit instability phenomenon can be relatively defined as unwanted and self-started signal oscillation. Stability is always an important issue for any linear system encompassing both signal gain and feedback. Common examples of a feedback system include the versatile opamp circuits and DC-DC converters.

A circuit with digital logic outputs, such as a voltage comparator, is of no instability concern, because it generally has no feedback, nor is it a linear circuit. Though positive feedback is often introduced into a comparator for obtaining hysteresis, circuit's non-linear behavior eliminates oscillation, i.e., its rail-to-tail operation of output renders its small-signal gain to be zero.

Accomplishing circuit's stability is one of the most challenging tasks in sensor's design. Fortunately, there are good references dealing with the subject. However, it is often difficult for a reader to balance the trade-offs between theoretical and practical approaches. For instance one may find a literature either oversimplifies the theory with impractical assumptions or, in the other extreme, mainly presents the theory in an abstract realm of mathematics. To help sensors design engineers speed up product development, this article presents the circuit stability theory in a hands-on sensor development scenario, emphasizing numerical techniques along with discussions on lab-based approaches.

Circuit stability theory

Figure 1 displays an ideal circuit model, which is the same as used in reference [1], to elaborate the theory on feedback and stability. The input signal Si and the feedback signal β*So are summed by an adder, and through an active path (amplifier) with gain μ, to generate the output So. The system's close-loop gain A is related to amplifier's open-loop gain μ and the feedback transfer function β by the legendary frequency-domain equation,

$$A = \frac{So}{Si} = \frac{\mu}{1-\mu\beta} \qquad (1)$$

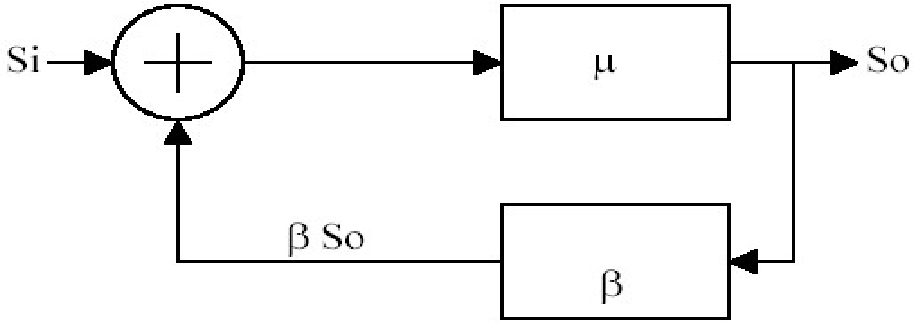


Figure 1

Figure 1. In this ideal feedback circuit, signals are transmitted in the direction pointed by the arrows. It is based on this feedback model that Equation 1 is derived for stability analysis.

Note that signal Si and So can be either current or voltage. This eliminates the necessity of discussing voltage and current feedback separately for our purpose. If we specifically define feedback to be negative, the denominator of Equation (1) would become $(1+\mu\beta)$, and the phase plot would accordingly have a 180° shift [2], [4].

If $\mu\beta=1$ (magnitude=1, phase=0), the system's gain A is infinite according to Equation (1) and the circuit is unstable and oscillates. The instability criterion, $\mu\beta=1$, corresponds to network zeros or natural frequencies. Oscillation can even take place in a negative feedback circuit, in which components' reactance introduces substantial phase shift to the feedback signal so that positive feedback actually occurs. At the frequency where $\mu\beta=1$, oscillation originates from noise or power-on transient at input, and is then amplified greatly at output. Oscillation is sustained as the output, via feedback, constantly drives the amplifier's input with zero input-output phase shift. To obtain stability, we prevent $\mu\beta=1$. In the linear oscillator design, however, we strive for $\mu\beta=1$ at the frequency where oscillation is desired.

In Equation (1) the term $\mu\beta$ is called the *loop gain*, which is solely responsible for a circuit's instability. It is important to keep in mind that the loop gain $\mu\beta$, the open-loop gain μ, and the close-loop gain A are 3 distinct parameters. The loop gain $\mu\beta$ can be physically interpreted with Figure 2. Other than a wire is broken, Figure 2 is the same circuit as in Figure 1. The reason for breaking the wire is to create a loop input terminal M as well as a loop output terminal N for test. If we can somehow produce an AC signal Vtest and the circuit will respond to generate Vreturn, then it is clear that $\mu\beta$=Vreturn/Vtest. Here the input Si is grounded for simplicity, because stability should be a loop quantity and independent of input. Note here Vreturn and Vtest imply voltages, but they can both be replaced with current signals without loss of generality.

The paradox here is that we still need the broken loop to function just like it is physically intact. To resolve this conflict, DC biases at M and N must be kept equal and remain the same as during normal operation. In computer modeling this can be done with a voltage source between N and M. In the lab measurement a resistor can be used to connect N and M to break the loop without disturbing circuit DC bias. The resistor value should be much smaller than those of other components. Now we can inject an excitation AC signal differentially between M and N. The circuit will react by adjusting Vtest (driving source) and Vreturn (loop response) according to the loop gain. Within the dynamic range of circuit operation, the ratio Vreturn/Vtest (loop gain) is independent of the AC injection magnitude due to the proportionality property of a linear circuit. Differing from the reality, however, there is an unlimited dynamic range in numerical AC simulation. Measurement of Vreturn/Vtest over frequency produces the loop gain Bode plots containing critical stability information.

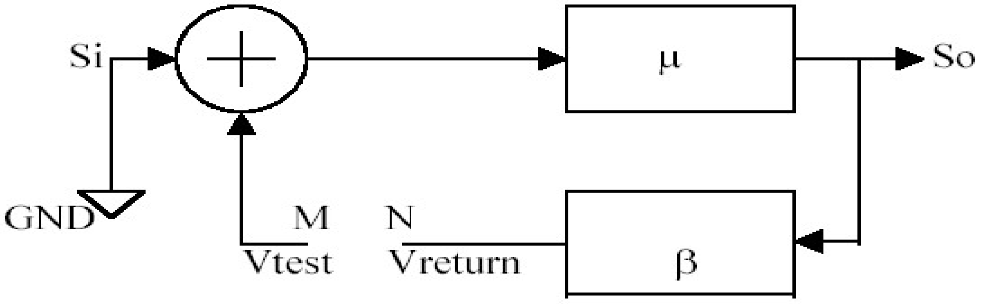


Figure 2

Figure 2. A wire of the ideal feedback circuit is broken for physical interpretation of loop gain.

A common misconception in studying circuit stability is to look at the open-loop gain μ or the close-loop gain A. Even though their plots appear similar to that of the loop gain, particularly when the feedback path is purely resistive, it is technically incorrect to use A or μ for stability analysis. This is also the root cause of my aforementioned faulty stability investigation. Despite the fact that only the loop gain contains stability information, studying A or μ is nevertheless beneficial. They reveal circuit bandwidth or speed, poles and zeros. Also the open-loop gain μ signifies if an IC is already internally compensated so that it is stable in most conditions.

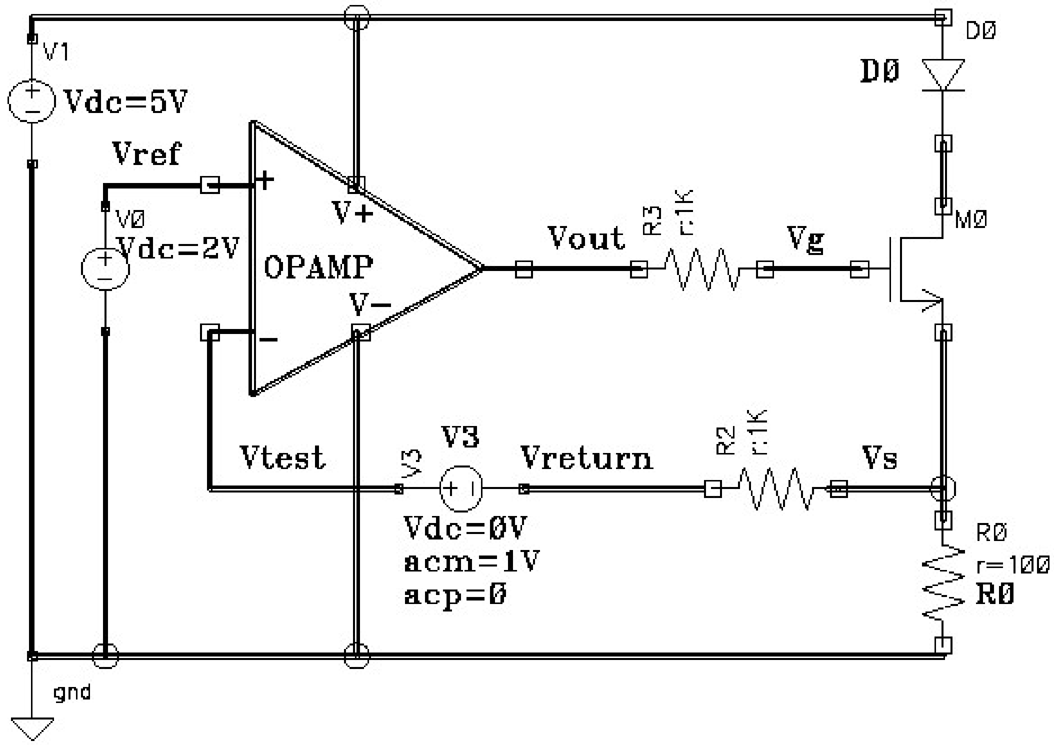


Figure 3

Figure 3. In this opamp feedback circuit, voltage sourceV3 is used to break the feedback loop for loop gain computation in AC analysis.

Normal loop gain derived by AC analysis

Figure 3 illustrates an example of circuit feedback. Through feedback, the opamp maintains a constant current through LED D0 with a value of Vref/R0. The analysis method used here is a direct application of the loop gain's physical interpretation (Figures 1 and 2). As the signal in the ideal circuit model is transmitted unilaterally (the normal transmission), the result is termed as the normal loop gain. By inserting voltage source V3 (DC=0V, magnitude=1V, phase=0) in Figure 3, we break the loop without altering its DC bias. After running one AC analysis using Cadence's Virtuoso Spectre Circuit Simulator, we manipulate simulation data to display the loop gain in Figure 4.

Phase margin is the loop-gain phase at the frequency where the loop-gain dB20 is zero (this is the unity loop gain or 0 dB crossover frequency). Gain margin is the negative of loop-gain dB20 at the frequency where the phase is zero. From the plots, phase margin is 76.7° at 2.88 MHz and gain margin is 16.7dB at 20.2 MHz. The circuit studied here has positive gain and phase margins and thus is stable. The unstable condition $\mu\beta=1$ translates into loop-gain dB20=0 and phase=0 at oscillation frequencies, which is clearly not satisfied in Figure 4. Note here that we can also break the loop elsewhere such as at signal nodes Vout, Vg, or Vs for a similar loop gain result with small but detectable discrepancy. Here we reiterate that only one AC simulation is performed in this section to calculate the normal loop gain. The limitation of this scheme is discussed later.

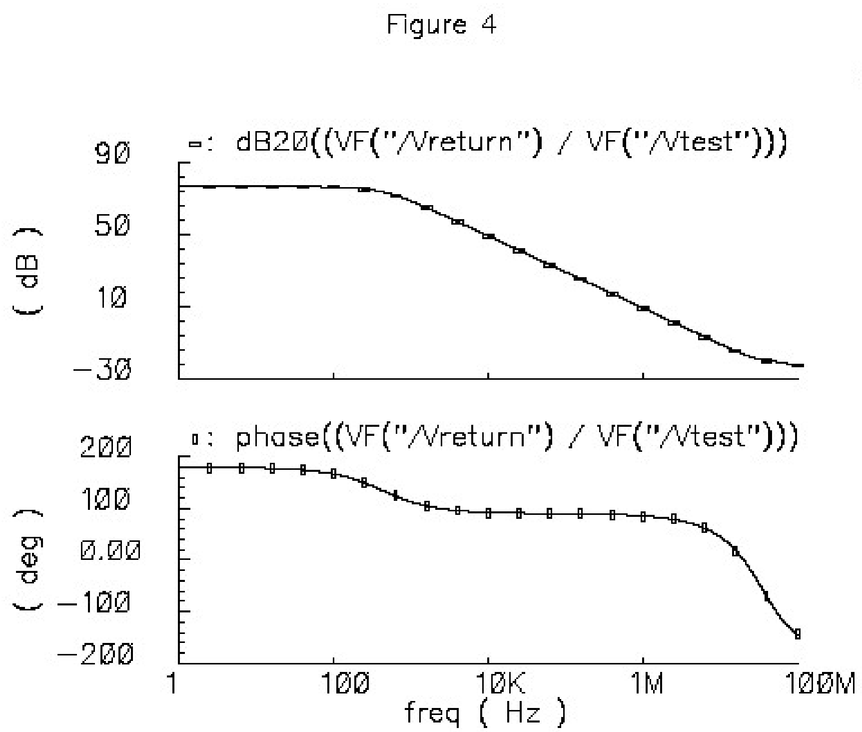


Figure 4., Loop gain amplitude and phase of the opamp feedback circuit are calculated and displayed using data from single AC simulation.

It is interesting to review Figure 5 for individual signals used to calculate the loop gain of Figure 4. Here VF indicates voltage in the frequency domain. They illustrate how V3's 1V AC is partitioned between Vtest and Vreturn and that signals obey Kirchhoff's law dictating that, in vectors, Vtest=V3+Vreturn. Here Vtest and Vreturn are referenced to ground.

AC simulation can actually provide all the information needed for stability analysis [M. Tian, private communication, April, 2005]. If we use a single AC analysis to calculate the normal loop gain as shown in Figure 4, then the location of the breakpoint is important, otherwise we can only derive part of the normal loop gain. The Middlebrook approach [1] calculates normal loop gain by using two-signal injection and two AC analyses to eliminate the need of choosing suitable breakpoint location. If we manipulate the data from two AC analyses using the formula in [1], we can derive the true loop gain, as further described in the following section.

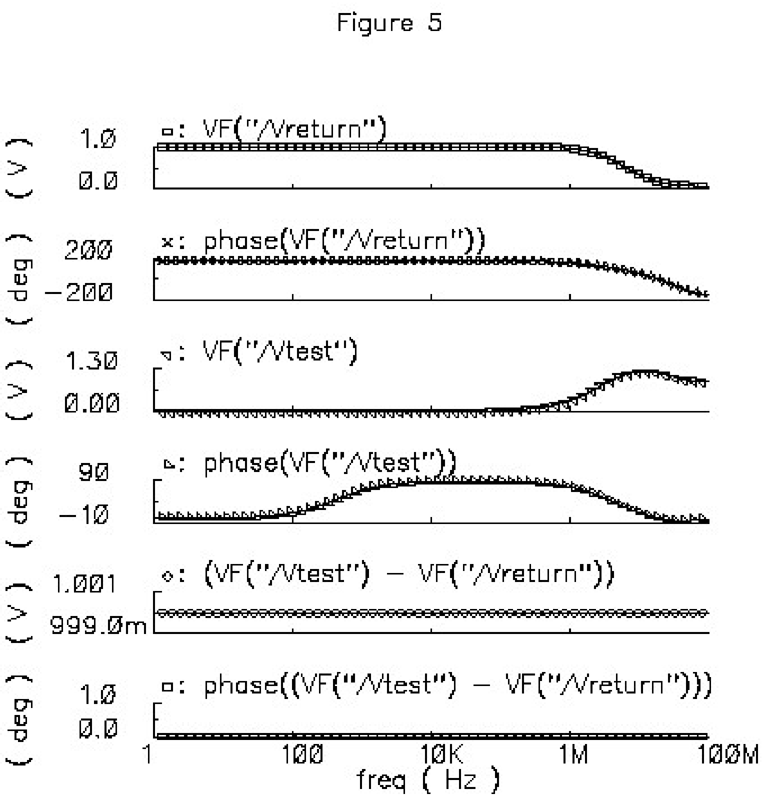
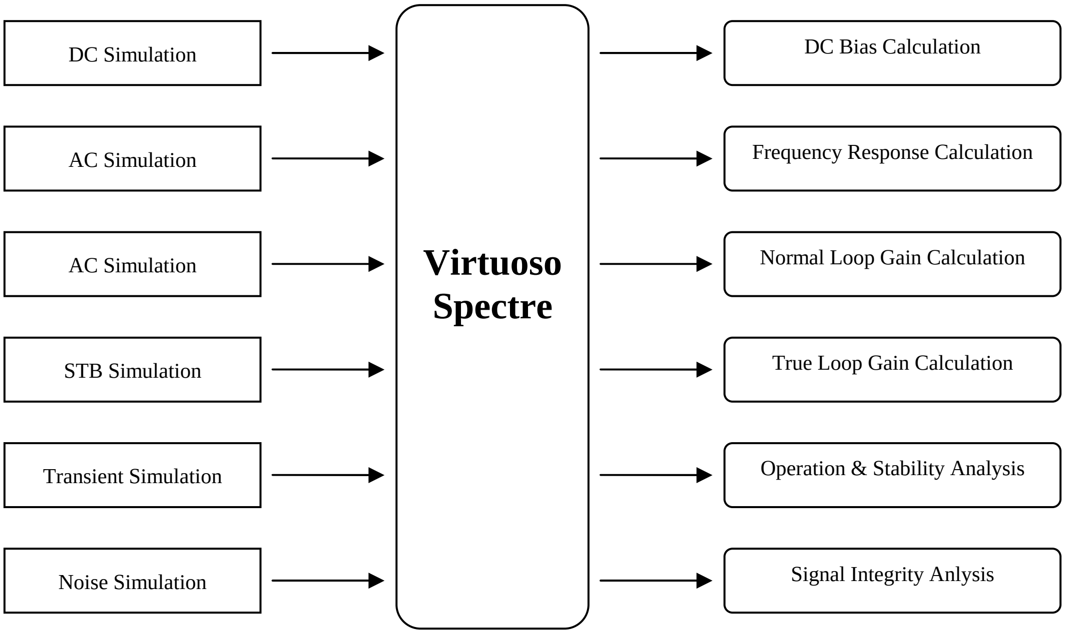


Figure 5. Individual signals used to calculate normal loop gain in AC analysis obey Kirchhoff's law.

Before we proceed to the next section, let's summarize what can and should be done with Virtuoso Spectre Circuit Simulator in the following simulation flow chart:



The stb simulation is the topic discussed below. Further simulation should be run for different temperatures and the worst manufacturing processes.

True loop gain by stability (stb) analysis

The most accurate stability algorithm calculates the true loop gain, which is the sum of the normal (transmission) loop gain and the reverse (transmission) loop gain [1]. Figure 1 is a normal loop gain model, which assumes that signal flows unilaterally through the loop in directions pointed by arrows. For stability analysis Cadence's Virtuoso Spectre Circuit Simulator extends the model of Figure 1, among other things, to include signal reverse transmission, which is significant at high frequencies [1], [3]. In the stb analysis, the simulator first deactivates the network inputs, then injects both test current and test voltage simultaneously and measure circuit AC response. With two such separate AC analyses the simulator is able to characterize the circuit parameters. It is based on these parameters that the loop gain is calculated. This scheme effectively cancels out any influence of breakpoint location on DC impedance, so we can break loop anywhere with the same result.

To obtain the true loop gain numerically, we must run a separate simulation called stability analysis (stb) with Cadence's Virtuoso Spectre Circuit Simulator [3]. We now compute the true loop gain for the same circuit as in Figure 3. Though V3 is again used to break the loop in the new scheme, Cadence allows substituting V3 with an instance called Iprobe (To directly evaluate stability for differential input-differential output feedback network, or fully differential amplifiers, Cadence further offers a 4-terminal symbol called dmcmprobe.)

V3's amplitude and phase are not used (simulator injects test sources on its own). V3's polarity or location in the loop is not important either. In simulation setup, we are required to select V3 as the "probe instance" and specify the frequency range. After simulation the simulator displays phase and gain margins and automatically generate the true loop gain plots in Figure 6. Phase margin is 76.8° at 2.90 MHz and gain margin is 16.7 dB at 21.4 MHz. As suggested in Figure 4 and Figure 6, the loop gains derived from a single AC simulation and from the stb simulation are consistent at low frequencies, with obvious discrepancies at high frequencies mostly due to signal's reverse transmission.

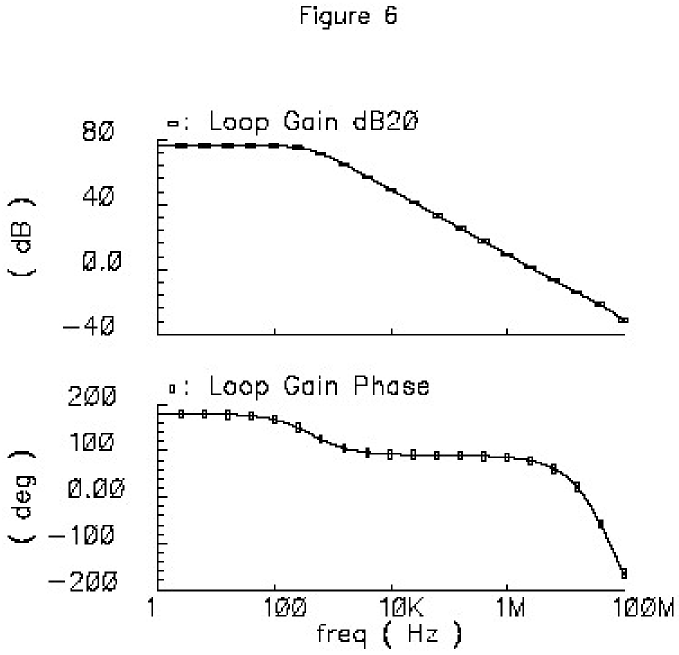


Figure 6. In the stb analysis the simulator automatically generates true loop gain Bode plots.

Discussions

The first scheme, using a single AC simulation to derive the normal loop gain, generally has the following drawbacks or limitations. (1) Results tend to depend on the type and location of the input. In Figure 3, V3's intrusion can impact the opamp input coupling, which correspondingly modifies the circuit operating point and compromise consistency of loop gain computations among using different breakpoints. (2) We assume the signal transmission is unilateral. This assumption causes errors at ultra-high frequencies, because both the active path and the return loop are generally bilateral. (3) The key to calculate an accurate normal loop gain is to select a suitable breakpoint without disturbing the loop DC bias. To this end, the specific feedback configuration needs to be pre-identified before simulation. For example, the circuit in Figure 3 is in the series-shunt feedback configuration because the feedback network is connected in serious with the input and shunts the output [4]. Unfortunately this suitable breakpoint is often not obvious or may not exist at all in a realistic circuit, where the input, output and feedback networks can be very complicated.

The second scheme, the stb simulation, has the following advantages [1]. (1) It calculates the true loop gain (normal plus reverse) with the highest accuracy. (2) The simulation setup is extremely easy and the breakpoint can be anywhere in the loop. (3) We do not need to identify μ and β, nor do we need to identify the type of the feedback configuration. (4) It does not matter whether we view voltage or current as signal of interest, and simulator will produce the same loop gain.

How much phase and gain margins shall we need to guarantee a circuit’s stability? It depends on what degree of signal integrity is required, or how much signal overshoot/ringing can be tolerated, though a 45° plus phase margin and a few dB's gain margin is generally acceptable.

What we have shown in Figures 1-3 is a single return loop circuit and covered by Bode’s single-loop theory. When designing a multi-loop feedback circuit, if we can identify a critical wire to break all the loops, only one simulation or measurement is sufficient. If such a critical wire is not available, we must study each loop separately to ensure all of them meet the stability criterion. This gives the necessary condition for overall sensor’s stability. It is also important to note that wherever possible, parasitic parameters should be included in loop gain calculation along with load (real and parasitic) parameters. Special tools may be required to extract information for parasitic components.

In complementary to the loop-based stability analysis described above, Cadence;s Virtuoso Spectre Circuit Simulator supports a device-based algorithm for evaluation of local loops [1], [3]. An example of local loops is a single transistor circuit, where parasitic junction capacitance can form local feedback loops and cause instability at ultra-high frequencies. A realistic circuit generally contains both global loops (loop-based algorithm) and local loops (device-based algorithm). The loop-based algorithm determines the stability of the overall network as long as the local loops are stable. The device-based algorithm is not often important to sensors, which generally work in frequencies lower than those where local loops’ instability is troublesome.

Time-domain and lab-based approaches

After the loop gain stability analysis, time-domain numerical and/or experimental approaches should then be used to cross-examine the circuit based on the following considerations and tips:

- Application conditions can be different from the ones used in frequency-domain stability analysis. Time-domain numerical simulation or bench test is helpful as there is correlation between poor phase margin and overshoot/ringing in transient signals. We can perform test by using a current pulse at output to start oscillation and see how it attenuates. A conditional stable or unstable circuit cannot suppress the induced oscillation and should have large overshoot in respond to signal transient. Similarly, we can check stability by power cycling the circuit to see if signal’s overshoot/ringing is acceptable.
- The numerical simulation scheme presented above is limited to diagnosing analog circuits, where circuit operation is linear and signal is small AC around its DC bias point. We cannot use the AC (or stb) simulation method for a system with logic control; even the whole system’s operation is in the small-signal region. This is because the logic output is at power rails so that the small-signal loop gain is nullified and stability simulation is invalid. Therefore for a linear system with digital control, the loop gain cannot be analyzed as is with numerical methods, but instead can be measured directly in the lab. A popular lab approach is to use an instrument called frequency response analyzer [5]. The instrument operation is based on the loop gain physical interpretation as shown in Figure 2. With adequate selection of break point and injection method, this lab method is a good approximation to the true loop gain.
- There are always parasitic loops and signal inter-trace crosstalk that may not be practically characterized. Therefore good layout practice is equally important. Keep noisy signal traces away from amplifier's input and other high-impedance analog nodes. Separate digital and analog grounds. Plan carefully for noise shielding, decoupling and EMI control.
- We may encounter high-frequency signal degradation due to device’s local loops, which are not accessible at the circuit level. Here experimental evaluation of product stability may become necessary. Remember also we have the option of invoking the device-based algorithm for stability study.
- Whenever the gain or phase margin is not favorable or excess overshoot is observed, the frequency compensation techniques (using RC network in the loop) should be implemented. An RC filter introduces a pole in the loop gain and produces more phase margin if used properly, though at the price of reduced circuit speed.

References

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Trademarks

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