# A PCELLS Library and Routing Tool Giving Designers the Option of a DFM Approach

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# A pcells library and routing tool giving designers the option of a DFM approach.

The idea of conceiving a DFM compliant parametric cells library came as a result of the awareness of a missing link between the traditional design approach and manufacturing needs.
Therefore its implementation was not as usual the result of current customers' requests, but an attempt to introduce new pcells features which could stimulate designers to begin to consider the adoption of a new design approach at gate level.
A first consequent objective was : let this new approach to be perceived by customers/designers not as revolutionary in its outer form so that it can be naturally and gradually adopted.
The designer should in fact easily move towards it by finding in his/her library pcells, optional and new functions close to those parameters that he/she is for a long time accustomed to use.
A designer does not need to move a specific separate DFM Design Kit or pcells library , but just to go on using a process focused Design Kit as usual :he/she would always been given the option to choose case by case during the phase of schematic entry either a "all minimum sizes" pcell or a pcell where some sizes might be relaxed and become larger in order to meet ,when possible, DFM requirements.
Another objective was : let the original level of complexity of pcells remain intact ; they have in fact several functions beyond the necessary length and width parameters, and all those functions should be kept.

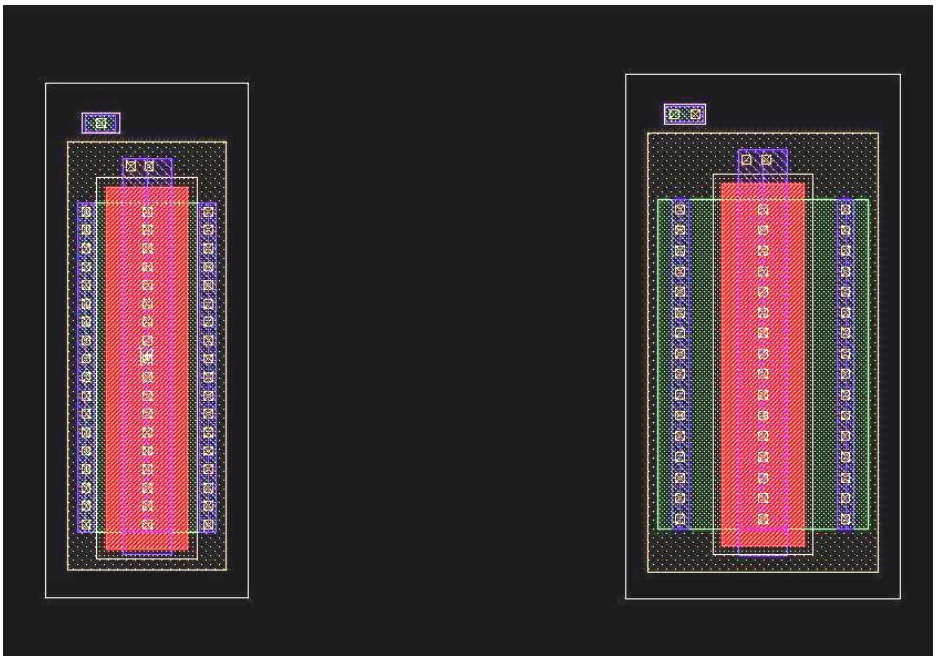
Such a target to go on offering designers a familiar library and tool, has of course on the other hand limited from the beginning the variety of possible solutions to implement in order to introduce a DFM approach at gate level. It came in fact as a consequence that only Skill procedures responsible of the generation of the pcells layout views could be amended together with the CDF files associated with their symbols and this change needed to be merely an integration.
Another limit came from the fact the new DFM oriented functions would in no case affect the already present traditional functions, but naturally marry them.
At the moment of the schematic editing in the Virtuoso XL environment, a designer should therefore find just some new parameters inside the form of "Edit object properties" which is associated to a symbol.

Standard pcells in my Design Kit libraries are traditionally created with Skill language and ROD macro-functions ;they are meant to lead ,through their inner connectivity information, to an automatic routing after placement.
Transistors pcells foresee the function of automatic abutment and the generation of multiple gates structures as well. Most of them have four terminals, their layout structure includes then the presence of a bulk.
Their traditional functions include a "threshold value parameter" which is responsible of the generation of the number of gates : whenever the chosen value for the transistor width is bigger than that of its threshold value, a structure with multiple gates is created .
Other six parameters rule all contacts generation. One parameter allows to decrement their number; When they are decreased , a parameter is responsible of their vertical alignment with respect to their active area .Other two parameters work independently and enable/disable the presence of all source / drain contacts ; a fifth parameter allows to create contacts between gates and another enables the optional presence of a structure for a bulk terminal.
This choice of functions for transistors pcells came for a long time as the result of the requirements from designers in various processes and it has been up to now kept as our standard .

According to the indications of our process development team ( in this case a 0.13u CMOS technology ) , the DFM oriented transistor pcell had to foresee larger contact – to – contact distance, longer extension of the gate structure outside the active area, larger drain / source areas together with flexible horizontal contacts position. The active areas extensions could eventually also be asymmetrical. Besides , its fourth terminal structure should have at least two contacts. Anyhow it should be evident to the designer at the moment of the instantiation of a cell that he/she is asking for an alternative structure, of DFM type.

It has been introduced a general parameter that enables the pcell to assume DFM features ; afterwards a designer can choose between these features : to have more spaced contacts or larger active areas or both of them.

When a designer chooses to adopt “DFM contacts”, the resulting pcell layout has both larger vertical distance between contacts (the minimum distance value is increased by a fixed percentage ) and larger extension of the gate outside the active area. The augmentation of these lengths has been up to now kept fixed and not editable by the user in order to avoid to give place to uncorrect layout structures according to the design rules .
When the choice falls on having bigger source / drain areas, percentage values representing the increase of the present areas should be instead introduced ,between 0 (default) and a maximum value . Drain and source increase parameters work independently so that eventually also an asymmetrical transistor can be generated.
In case of considerable growth of the active areas, being the original position of their contacts unsuitable, they can be horizontally shifted in a flexible way via two independent editable parameters. Their default value of 50 per cent corresponds to the position of contacts centrally placed with respect to their resulting active areas ; the value of 100 places them instead on the farthest side from the gate.



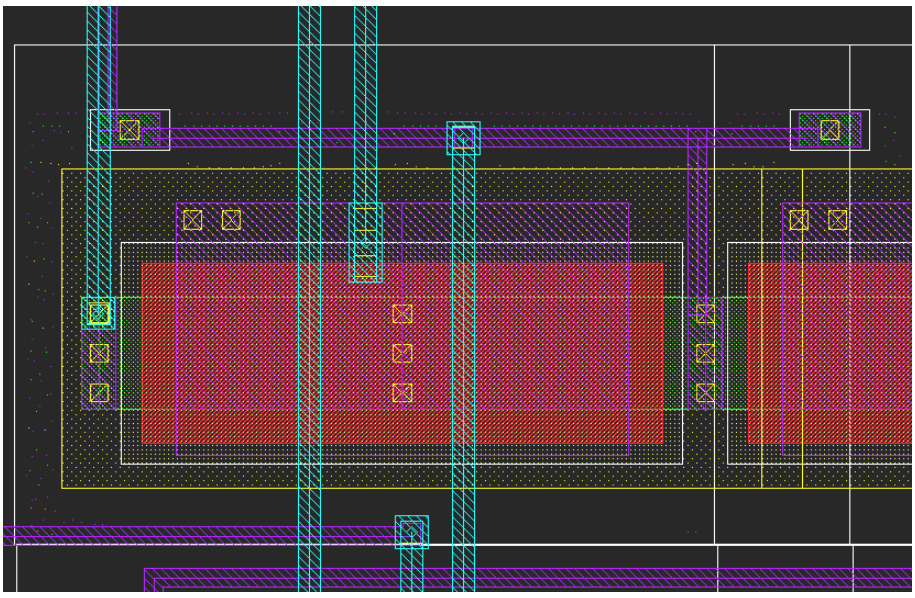
The picture shows details of pcells layout views : on the right the DFM transistor , while keeping the same values for width and length of the “standard” one ( on the left ) has evident bigger drain and source areas which have been increased of 80 % with relative contacts moved from their original positions and double contacts in the bulk active stripe. Due to the scale factor, bigger vertical spaces between source/drain/gate contacts as well as larger gate extension outside the active areas are difficult to see ; the global slightly increased vertical dimension of the cell is the result of the latter.

An easier adoption by designers of a DFM approach at gate level has passed through the demonstration that this approach is possible without compromising the whole chip area density wherever it is locally feasible to have just some more space to adopt a DFM cell together with appropriate routing guide lines.

Due to the fact that on one hand our designers are ever more invited to make use of the iccraftman tool as a mean for automatic routing, and on the other hand DFM oriented pcells make sense only when they are conjugated with a coherent routing, an effort has been done to offer designers a customized version of the tool iccraftman which could cope with a DFM practise.

I adopted the choice of having only one “rules file” to be used during the export of a layout to router, together with two alternative and optional start-up “do files” versions : a “do file” suitable for the traditional approach of making the whole chip area as small as possible and another one for a DFM oriented design.
The aim of the “standard approach” “do file” is linked to the requirements of the process in question : to set an interlayer clearance between the routing poly layer and a “frame” layer of the transistor structure. The purpose of the optional DFM do file is also to improve interconnect reliability, that means relaxing both the minimum spacing rules and the minimum width rules for metal connecting layers. The file is also meant to improve the via reliability by using double contact vias ,which can be used for any interconnect pair by specifying in the rules file a via array template for a layer pair and then by defining in the DFM do file a class for the nets that will use double cut vias and then setting a “use_via” circuit rule.

To dispose of a concrete mean of verification of the usefulness of the customized iccraftman generated files, designers were asked to provide with a significant portion of a chip they were developing in the same technology .That means a circuit where both all low voltage and high voltage transistors were foreseen, with different dimensions, parametrical functions values and possibly also with more than one gate. From its original schematic view, another schematic page was derived by making any instantiated symbol to point to the respective DFM pcell component.
In this page various combinations of DFM parameters values were introduced , keeping in any transistor the active areas increases significant, although not excessive so that the whole chip area did not need to dramatically grow and therefore the comparison between the starting conditions of the two layout views could be meaningful. The global dimensions of the two layouts were in fact very close : 62.3u x 58.64u in the case of traditional pcells layout and 73.3u x 60u in that of dfm-oriented layout. This proved to designers that it is possible to make use of a global DFM approach ( pcells technology library and automatic routing ) without significant loss of chip density.
In the two corresponding layout pages ( automatically derived from their schematics ) the ( manual ) placement of components was done taking care of keeping the relative correspondence of their positions as conservative as possible in order also to let the routing tool start from two similar layouts so that variations in the connections could be mostly put in reference with the different aspect and size of the pcells .
Continuous iterations and consequent calibrations of both the rules file and the optional “do files” had first of course the objective of reaching a routed layout with all necessary connections on one hand and that could be on the other hand clean with reference to the process design rules and these calibrations have also led to a final and suitable form for any file implied in the automatic routing.
These calibrations were meant not to be tied to the specific layouts in question , but as general as possible so that the files could be extended to any other design layout in the same technology and therefore in the next future by designers working with this technology.



The picture above shows a detail of the layout page using standard pcells; the picture underneath the corresponding area in the DFM layout.
Obvious differences are: the pcell bulk area which has two contacts in the second layout and the horizontal increase of the active areas with a new position for their contacts which are now more vertically spaced and less close to the gate.
The routing in the first picture also shows in the gate area a metal1 to metal2 via using two contacts. As requested by the concerned technology rules in fact, big metal1 gate area ( transistor widths greater than 1.4u ) should always be accessed by more than one contact .The optional “do files” developed for the export to the iccraftman environment from the Opus environment , have implemented such process request.