

Automated Custom Physical Design (ACPD) Flow In CADENCE IC5.0.x For Mixed-Signal Designs

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ABSTRACT

The ACPD flow is vital for accelerated mixed-signal layout design. This paper will provide the flow details, tools, and the steps involved. Automatic layout generation and connectivity extraction using standard cells for digital blocks will be explained. Automatic placement is done using the Virtuoso Custom Placer(VCP). Advanced pcells are utilized for layout generation of the analog blocks. Virtuoso XL(VXL) features such as Show Incomplete Nets and incremental updates will be discussed. Manual area based placement is done for the analog blocks. The analog and digital blocks are routed at the device level using the Virtuoso Custom Router(VCR). Placement of these routed blocks is done at the top level in VXL. Critical Nets are pre-routed in VXL using the Wire Editor tool. Setup of the Wire Editor and its features will be discussed. Abstract views will be created for these layout blocks. The Cadence Chip Assembly Router(CCAR) is utilized for block level routing. The .do file setup and commands will be explained. Once the routing is completed the layout design is accomplished. The design is then imported back into VXL for physical verification.

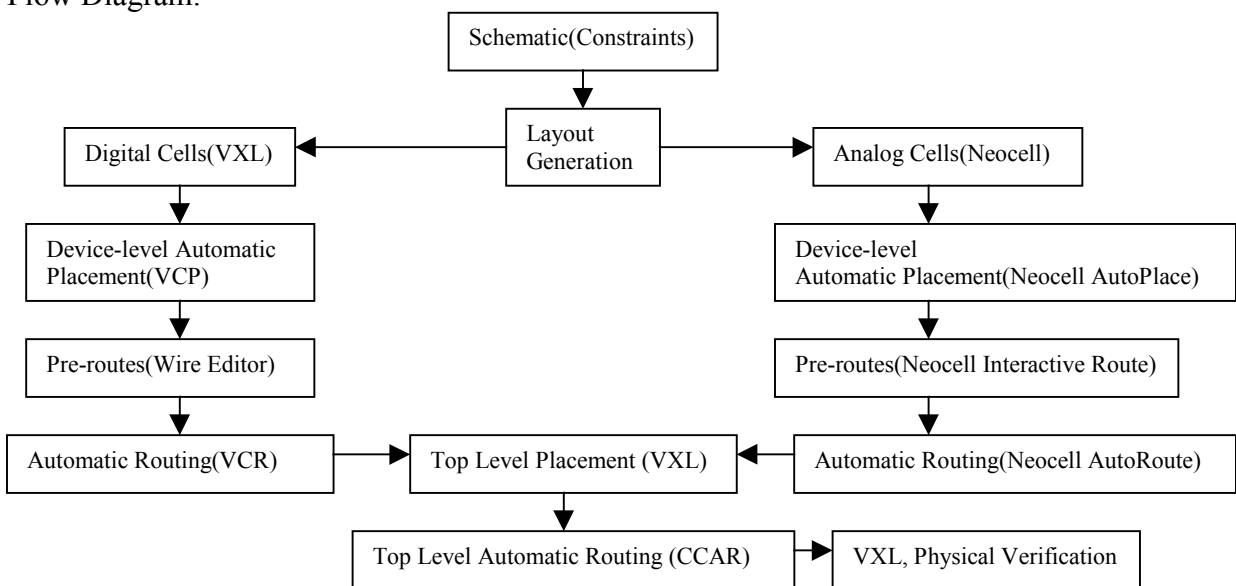
1. INTRODUCTION

The concept of system-on-chip(SoC) is an important segment in the market of integrated circuits. The recent developments have increased the number of devices and the functionality that can be put on a chip where these chips include both digital and analog circuits. Here I will address the topic of automating the layout design for mixed-signal designs. Automated Custom Physical Design (ACPD) flow is central to a mixed-signal layout design. This flow highly automates the layout generation and design process resulting in shorter design cycle time. The ACPD flow utilizes advanced parameterized cells (pcells), design rule driven editing environment, automated placement, and automated routing all in a connectivity based environment to achieve physical mask layout data.

2. METHODOLOGY

The methodology and the flow utilized help to solve the mixed-signal layout design issues. The tools utilized are primarily from Cadence Design Systems which have been customized for the National Semiconductor mixed-signal design CAD environment. The layout design for the digital block is done using schematic driven layout generation, Virtuoso Custom Placer (VCP), and the Virtuoso Custom Router (VCR). The analog blocks are then designed using pcells, Neocell module generators, and place and route using Neocell. The top-level layout is then generated in Virtuoso XL (VXL), placed, and then routed in the Cadence Chip Assembly Router (CCAR) tool. All the tools and flows are quite intricately integrated so that the designer does not have to spend too much time in translation, import, and export of intermediary files between different tools or vendors. The Cadence Virtuoso tools are primarily used in combination with Neocell, advanced ROD based pcells, and the Auto Router.

Flow Diagram:



3. DIGITAL BLOCKS

The top level schematic will generally consist of many blocks and symbols with wiring. The schematic for one of the digital blocks, a sub-block in the top level schematic, is opened. This schematic will have the completed circuit for this block. Constraints have to be added to the schematic. To facilitate this, the Virtuoso Constraint Manager tool is utilized.

3.1 Constraint Manager

The Virtuoso Constraint Manager enables the designer to define, manage, and transfer constraints throughout the ACPD flow. Constraints can be set on nets and instances. The constraints supported are NetBased, Distance, Alignment, Grouping, Symmetry and Fixed constraints. NetBased constraints set no-cross rules for nets and classes of nets. The width of nets and classes of nets can be assigned. The routing priority for each net can be entered. Differential pairs can be created. Shielded wiring can also be specified.

Besides the NetBased constraint, all other constraints fall under the category of Geometric constraints. For Distance constraint category, the vertical and horizontal spacing between components can be controlled. The alignment of components can be set for vertical axis and horizontal axis. A set of components can be assigned to a group. Grouping Constraints can be assigned for this group. Symmetry constraints for devices can be entered with respect to orientation and spacing. Lastly components can be fixed at a particular location during placement. Once the constraints have been entered in the Constraint Manager, the schematic is saved to attach the constraints.

3.2 Virtuoso XL(VXL)

The primary tool used for layout generation is VXL which is the Cadence Layout Editor and Layout Accelerator tool.

3.3 Layout Generation and optimization

To do the layout generation the VXL tool is invoked from the schematic. In the VXL environment the layout is generated randomly below the placement boundary area. The majority of these layout instances are standard cells. VXL extracts the connectivity from the schematic and attaches them to the standard cells. For the users convenience the connectivity lines or flightlines between the layout instances, if turned on, can be viewed in VXL.

3.3.1 Layout Features

During the design stage, if some changes are added to the schematic such as the addition or deletion of symbols or the change of symbol parameters, the layout in the VXL environment can be incrementally updated without affecting the existing generated layout. Another good feature that will be very useful is the Multipart Path (MPP) functionality. This feature can be used to create guard rings as a pickup region. This will

also be very useful to create isolation guard rings to separate analog and digital parts for noise and other optimizations. To create the different guard rings, a MPP template is generated in VXL. This master template can be reused many times to generate the same guard ring. The template can also be modified easily to create different types of guard rings and paths.

3.4 Placement

The next step is the optimized placement of the layout generated earlier. The VCP tool is used to do automatic placement. The VCP tool provides automated pin placement and primarily a row based placer for digital cells. The constraints entered earlier in the Constraint Manager that are supported in VCP are Distance, Alignment, Grouping, Symmetry, and Fixed.

The first step is to do the pin placement. For pin placement, in the VCP GUI, the designer selects a set of pins and assigns the location to be placed. The spacing between the pins can be assigned. Pins can also be fixed at certain positions as a hard constraint.

Secondly the preparation for placement of the instances is done. The Partition GUI is invoked. A partition can be created for each group of instances. This will keep the specific groups of instances separated by the partition as it pertains to the user and the particular design. Else all the devices could be placed in the same partition. Next the Placement Style GUI is invoked. For the style, the Assisted Standard Cell is selected. The region to generate the rows is specified. The number of rows can be specified or it can be left to the Placer to generate automatically. The spacing between the rows are entered. The appropriate Filler Cells are selected. The size of the power and ground rails are also assigned. The Calculate Estimates feature is activated. This feature, based on the inputs provided by the designer, generates the appropriate number of rows and the length of the rows in order to generate an optimized placement.

The final step is to do the placement. The Placer tool is invoked. In the Placer GUI, the appropriate settings are done. The option to have all devices placed is selected. The Placer Run is set to optimal. The Filler Cells option is turned on. The appropriate cctrules file is selected. The cctrules contains design rule information, vias and contacts defaults, and other routing related information. The default cctrules, developed by the CAD group, is utilized by the VCP tool to do the placement. The Placer is then activated. The placement speed is quite impressive. Depending on the cell size, the placement should be done fairly soon. If the placement is not satisfactory, the Placement Style GUI may be re-invoked to regenerate the rows and the Placer tool may be re-run to achieve optimized placement results.

3.5 Pre-routes

Once the placement is done, some pre-routes of critical nets are done in VXL. This is done either by using path stitching or using the Wire Editor tool. The Wire Editor

includes features such as design rule correct interactive routing and editing, pushing of nets while routing, reshaping of wire segments, checking existing routes for violations, and the compaction of routes. Once the Wire Editor tool is activated, any terminal can be selected to be routed and the Wire Editor will automatically complete a point to point route to another terminal at the shortest length possible. All the pre-routes can be completed accordingly. Once the pre-routes are done, the cctrules and the layout is exported to the VCR tool for auto route.

3.6 Virtuoso Custom Router (VCR) – cell level automatic routing

The VCR tool is an extensive and advanced cell-level router for analog and small digital designs. VCR includes on the fly DRC checking for routing layers, pushing of nets while routing, cross-coupled and differential pair routing, and shielded routing. It is a shape based router with an easy interface with the Cadence VXL tool. The user can use the pull down menus or enter the VCR commands in the command line. Alternatively, the VCR commands can be entered in a separate ascii file with extension .do. Running this do file will enable the VCR tool to route the design automatically based on the constraints and commands set in the do file. The typical setups in the do file are the grid size, routing directions for the routing layers, selection of routing layers, stack via setup, and the number of route and clean iterations. Once the route is complete and satisfactory, the design is imported from VCR back into VXL and saved for later use in top level placement and routing.

For all the digital blocks, the same steps used in the first digital block are followed such as the constraints being set using the Constraint Manager, layout generation using VXL and placement using VCP, and cell-level automated routing using VCR.

4. ANALOG BLOCKS

Open the schematic of one of the analog blocks. The schematic will have the completed circuit for that block. For analog cell layout generation, automated placement, and automated routing the Neocell tool is used.

4.1 Neocell

The Neocell tool encompasses a Constraint Editor to enter constraints and an automated analog device-level place and route engine to provide a productive environment for analog cell-level physical design.

The Neocell Technology files have to be developed by the CAD in order to use the Neocell tool. The technology files contain design rule information, necessary defaults, and module generators which will be used to generate the layout. Besides the technology files, in the Composer tool which is a schematic editor, the CAD group will need to setup the interface to the Neocell tool. This is done by adding a new pull-down

menu called Neocell. The Neocell menu will have the entries to invoke the Constraint Editor and the Neocell Layout Editor which will explained in detail later.

4.2 Constraint Editor

To enter the constraints for the schematic the Constraint Editor tool is utilized. In the Constraint Editor the appropriate Neocell module generators or pcells are applied for all the devices. In a pcell the layout is defined using the ROD skill constructs. Variables and conditions are used in order to change the properties of a specific layout instance. The Neocell module generators can manipulate the MOS fingers any possible way to establish a particular interdigitation scheme. Variants and arrays can be setup for all the module generators. Body contacts can be automatically assigned. For all the pins the pin size, location, and priority can be assigned.

Other constraints to be set are the Group Form, Symmetry, Wire Style, Location, Grouping, and Matching. For the Group Form constraint, special and multiple guard rings can be setup for groups of devices or partitions. Matching constraint sets up devices that can be matched for orientation, location, and distance. The Wire Style constraint controls the wire width of each net. Symmetry constraint sets up symmetrical placement and routing among devices. After all the constraints have been assigned a Check feature can be activated to check for any errors or conflicting constraints. The constraints that are applied to the schematic are utilized later by Neocell to optimize the placement and routing of the layout.

4.3 Neocell Layout Editor

The schematic with the constraints is exported to the Neocell Layout Editor. In the Neocell Layout Editor the AutoPlace tool is activated which then completes the automated placement. Once the placement is done, if necessary, interactive placement by the designer may be done. Interactive placement can also be used to pre-place and fix important devices before running the AutoPlace tool. As in AutoPlace device merging and abutment, device orientation change, and latchup protection can be done in interactive placement. To fix DRC errors generated due to interactive placement, the convenient Fix DRC feature can be activated. This will automatically fix the DRC errors in the layout.

AutoRoute is an automatic device-level routing tool that provides symmetric routing. Once AutoRoute completes, if necessary, the interactive route feature is enabled. Controlled routing, Point to Point routing, Guided routing, and path stitching can be done. Wires and segments can be deleted, re-routed and notches can be filled. Once the design is placed and routed satisfactorily, the design is saved. This will automatically save the design into the Cadence layout database. The newly saved design from Neocell is then opened in VXL. Similarly all the analog blocks in the top level schematic are placed and routed using the above flow which utilizes the Neocell Constraint Editor and the Neocell Layout Editor.

5.0 TOP LEVEL

Once the layout design of all the digital and analog blocks are complete, the layout design for the top-level schematic is done.

5.1 Abstract Views – Analog and Digital Blocks

Abstract views need to be created for all the blocks. To create the abstract views, the Cadence IC5.0 Abstract Generator is invoked. For each block the Pins Step, the Extract step, and the Abstract step need to be completed in the Abstract Generator. This will generate the Abstract view which will be used later for top level routing in the Cadence Chip Assembly Router (CCAR).

5.2 Virtuoso XL(VXL) – top level

The top level schematic is invoked. From the schematic the VXL tool is invoked to do the layout generation.

5.2.1 Pcells

Critical to layout generation and automation are pcells. As mentioned earlier a pcell is a layout instance which can be programmed with several parameters as specified by the user. Pcells can be graphical or skill language based. At National Semiconductor the pcells are generally developed in the skill programming language. Advanced pcells are developed using Relative Object Design (ROD) constructs. Advanced pcell features include automatic abutment of transistor diffusion regions, pcell stretching, and path chopping. Mega-pcells, which is a pcell with more than one level of hierarchy, can be created for analog blocks such as cascode devices and differential pairs. The benefits of pcells is that they are highly flexible as parameters can be added, deleted, modified, and for mega-pcells the preferred routing could also be included. The pcell instances are always design rule correct. Pcells enable schematic driven layout generation and design.

5.2.2 Layout Generation

In the VXL window all the individual layout instances(pcells, standard cells) for the symbols as well as the analog and digital blocks designed earlier are generated. Each of the blocks and devices will have the connectivity associated towards each other which is extracted from the schematic. Placement of the generated blocks and devices can then be manually done by the designer inside the placement Boundary area. The cctrules file used by the CCAR tool with default settings is developed by the CAD group for the designer. The cctrules contains information about routing layers, vias and contacts, and other VXL related translation information for the CCAR tool. In the cctrules a keepout is added for the prBoundary “boundary” layer for all the routing layers. The prBoundary “boundary” is the layer that encompasses each of the abstract views that were created earlier. The purpose of adding this keepout into the cctrules is to avoid any routes over

the prBoundary “boundary” layer. This is done to avoid shorts as the block inside the prBoundary “boundary” has already been routed earlier.

5.3 Pre-routes

In VXL, at the top level with all the blocks and devices being placed, the pre-routes of critical nets is completed by using path stitching or by using the Wire Editor tool.

5.4 Cadence Chip Assembly Router (CCAR)

The CCAR tool is an extensive and advanced chip level router primarily for analog designs and small digital designs. The CCAR is similar to VCR in terms of the GUI and the usage except that the CCAR has the global routing and power routing capability.

From VXL, which has the top level placement, the CCAR tool is invoked. The design as well as all the layers and routing information from the cctrules is translated into CCAR. In the CCAR tool, similar to the VCR tool, the user can use the pull down menus, enter the CCAR commands in the command line or the commands can be entered in a do file. According to the designer’s discretion, before running the do file, the CCAR Compaction tool can be activated. This will compact the design blocks in the horizontal and vertical direction with respect to the design rules. After compaction, running the do file will enable the CCAR tool to route the design automatically based on the constraints and commands set in the do file. If the number of unconnects is high, the user can do some interactive placement or improve the do file to enable CCAR to complete the routes. Else the placement of some blocks or devices could be changed to enable the router to complete the routes. Especially for large designs if a high percentage of the routing could be automated, this would save a lot of layout design cycle time. Also iterations due to design rule violations, shorts, and layout optimization can be reduced.

5.5 Import to VXL

Once the route is completed in CCAR, the design is imported back into VXL. In VXL further clean up and routes may be done if necessary. Also more changes could be added to the design and re-exported back to CCAR for further routing. After the final routing the design is then re-imported back into VXL. These iterations can be done continuously, in conjunction with physical verification, until the designer is satisfied with the top level routing. This should result in the final layout.

6. CONCLUSION

The flows and tools discussed play an integral part in the layout automation of mixed signal designs. Going forward the integration of the tools, new features, and their enhancements could be encouraged. Some of the future developments could be that a) the VCP tool could provide the designers more flexibility in determining the placement area b) the VCP tool’s Engineering Change Order (ECO) flow could be enhanced for

schematic entry changes c) a more advanced Compaction tool is utilized for device level and block level compaction. With the current layout automation tool features, the ongoing expansion of pcell features and their complexity, and the possible future tool enhancements designers will be able to achieve a greater percentage of layout automation.

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